Insight And Validation of DP 2.0 and HDMI 2.1 Display Standards

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KEYSIGHT TECHNOLOGIES

Part 1 Agenda：DisplayPort

- General Introduction to DisplayPort
- Standard Committee and Compliance
  - DisplayPort Source Test Solution
  - DisplayPort Sink Test Solution
- Test Solution

General Introduction to DisplayPort

General Introduction to DisplayPort

REVIEW OF DISPLAYPORT

- The DisplayPort standard is administered by VESA[1].
- Introduced in 2007.
- Graphics interface from GPU to Display through external cable.
- DP technology addresses embedded models as well.
- Up to 4 forward differential lanes with fixed data rates.
- Can daisy chain up to 32 monitors.
- Connectors
  - Standard DP
  - Mini DP
  - USB Type-C

1. Video Electronics Standards Association

General Introduction to DisplayPort

REVIEW OF DISPLAYPORT INTERFACE

Main Link

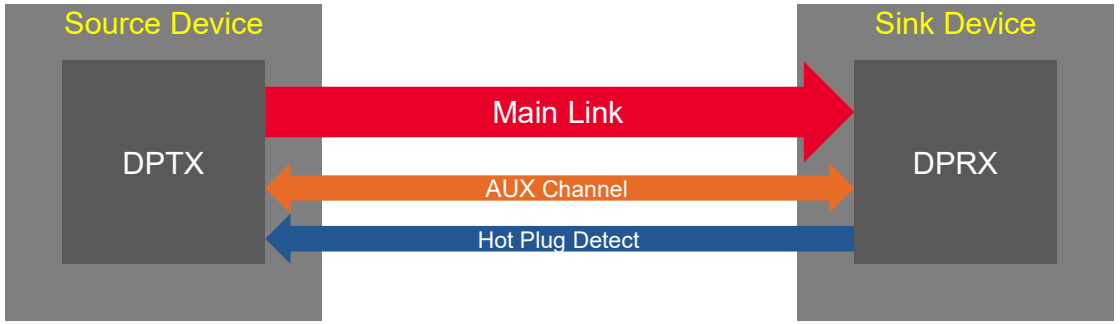
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

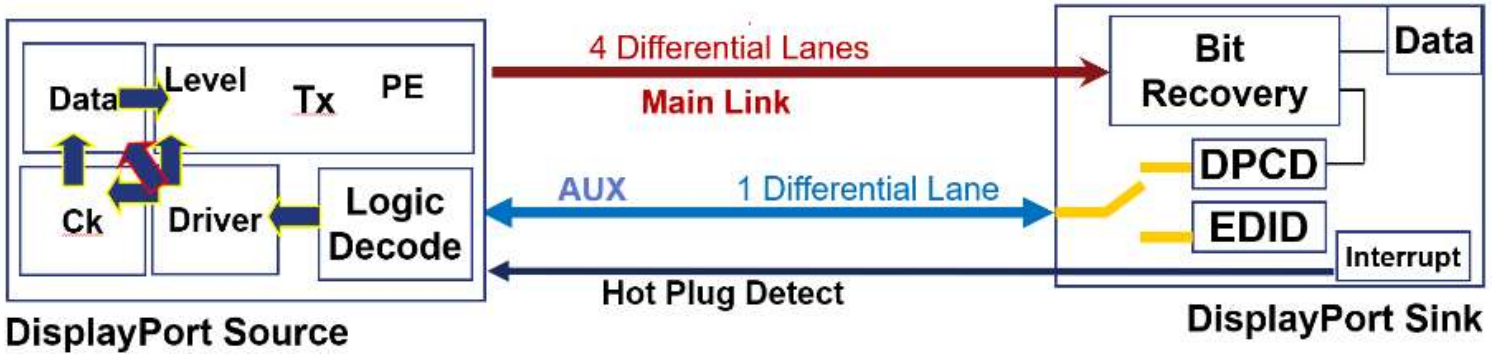
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



General Introduction to DisplayPort

REVIEW OF DISPLAYPORT INTERFACE



Main Link

- Up to 4 differential lanes: 4 possible bit rates
- TX:
  - 4 possible level settings
  - 4 possible pre-emphasis settings
  - Spread Spectrum Clocking (optional)
  - Dual Mode optional
- RX:
  - Receiver individual clock recovery
  - Receiver Tolerance curve specified.
  - Receiver Sensitivity = 50mV

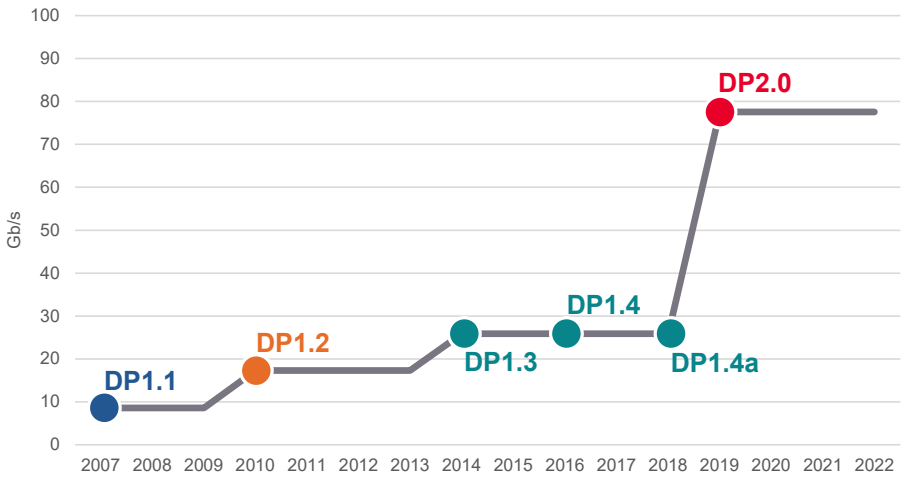
AUX Channel

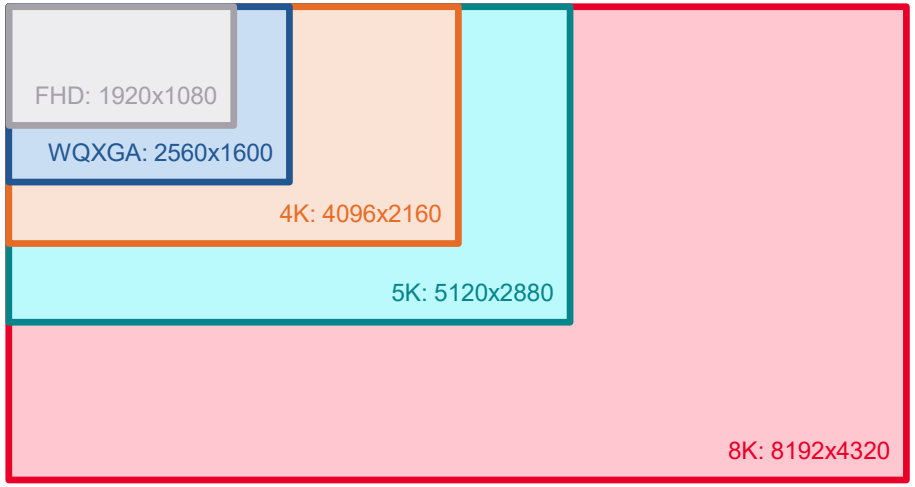
- Phy Layer
  - Bit rate at 1Mbs
  - Manchester II encoded
- Purpose
  - Link Management
  - Test Mode control

General Introduction to DisplayPort

MAXIMUM DATA TRANSFER RATE AND RESOLUTION

Aggregate Bandwidth



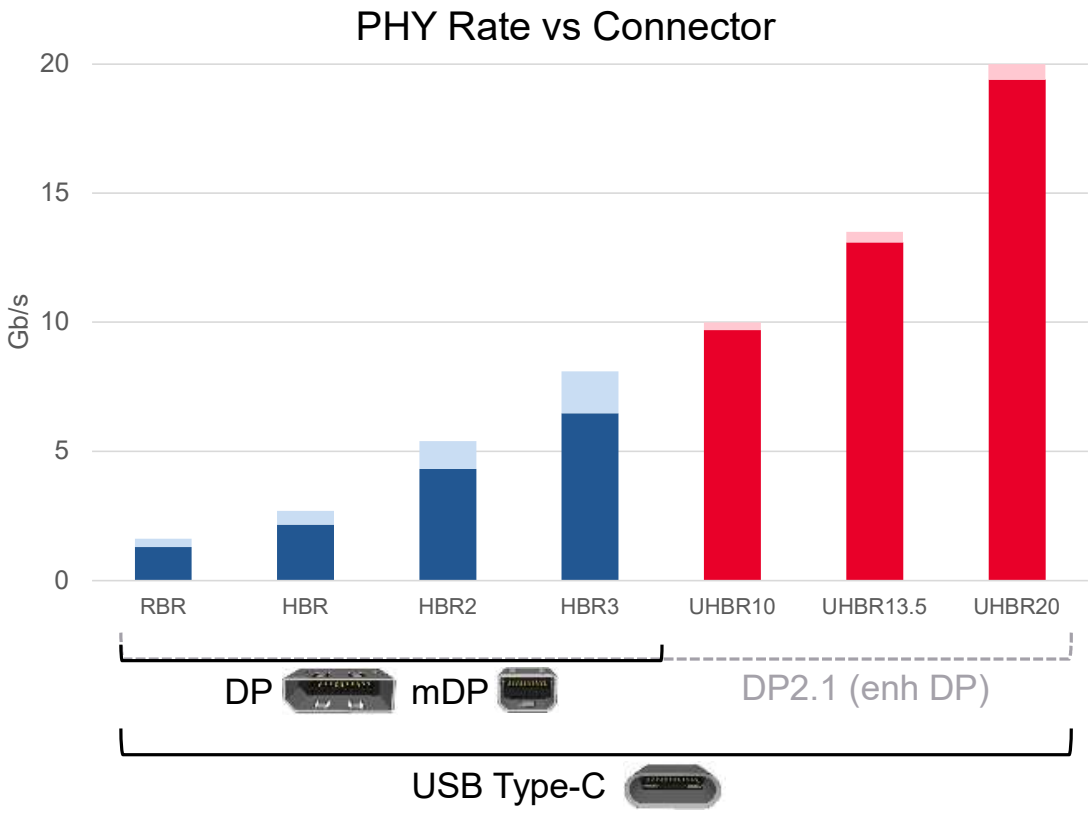


[1]Color depth = 24 bpp, refresh rate = 60 Hz

General Introduction to DisplayPort

PHY OVERVIEW – MAIN LINK

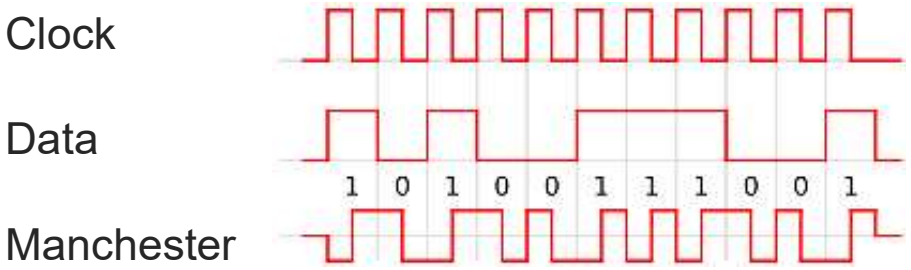
- One, two or four differential lanes
- Seven PHY rates(UHBR10, 13.5 and 20 Gb/s)
- Optional SSC
- RBR, HBR, HBR2, HBR3
  - 8b/10b coding → 80% efficiency
  - **4 voltage swing levels / 4 pre-emphasis levels**
  - RX EQ
- UHBR10, UHBR13.5, UHBR20
  - 128b/132b coding → 97% efficiency
  - **16 TX FFE presets**
  - RX EQ



General Introduction to DisplayPort

PHY OVERVIEW – AUX CHANNEL

- Half-duplex, bidirectional
- Doubly terminated, AC-coupled
- Manchester-II encoding
- 1 Mb/s, transactions < 500 µs

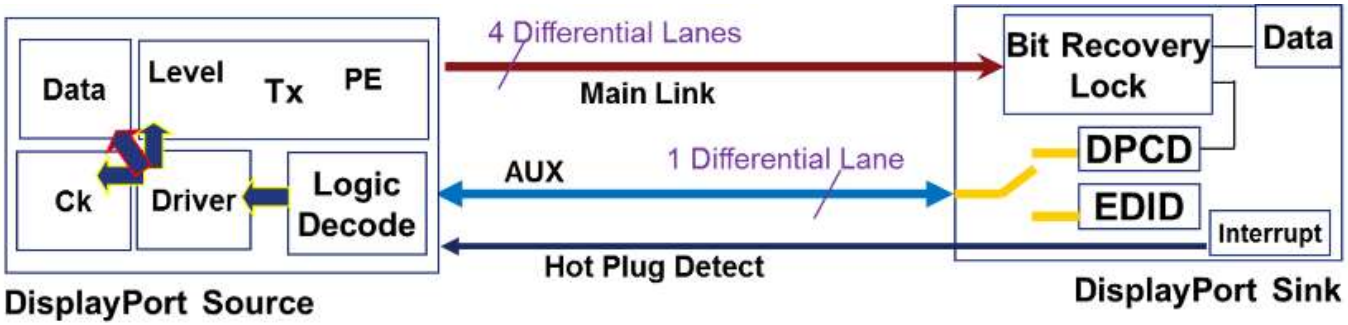


- Source is the Master, Sink is the Slave
- Link services
  - Rx capability discovery
  - Link initialization, maintenance
  - Link quality test support(test patterns)
- Device service
  - Sink event notifications
- Source detection by Sink(examine CM voltage)

General Introduction to DisplayPort

DP: SOURCE AND SINK COMMUNICATION OVER AUX

- HPD used for link connection as well as for link service.



- Connection:
- Source ‘sees’ connection: HPD high = sink/cable connected
- Source then reads the EDID data: Know preferred capability
- Source then reads DPCD (00h-FFh): Know DP capabilities
- Source will set up highest bit rate, lowest level on lanes and starts link training process.
- Sink updates link status on DPCD registers.
- Source reads DPCD values evaluates results to either progress through training, change level, pre-emphasis or bit rate

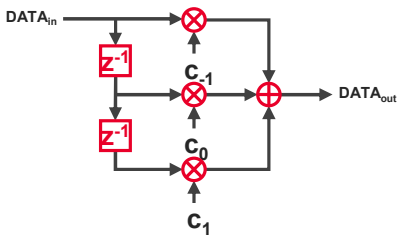
General Introduction to DisplayPort

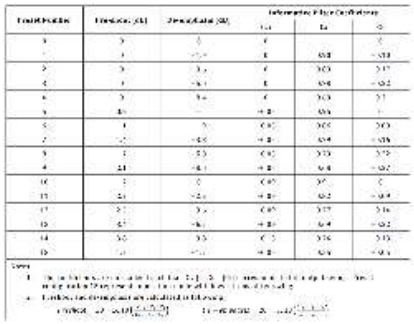
DP 2.0 SPECIFICATION: EQUALIZATION

- DPTX: 3-tap FFE (16 Presets)
- DPRX: CTLE (10 DC gain levels) + DFE
- Full characterization: 16 x 10 = **160 combinations**

DPTX

3-tap FFE, 16 presets

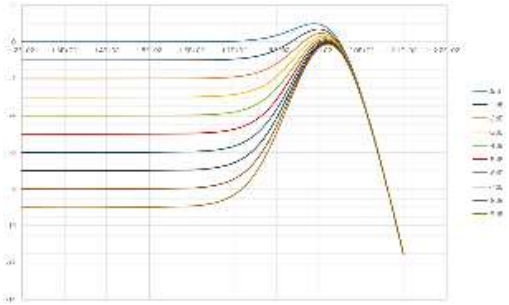


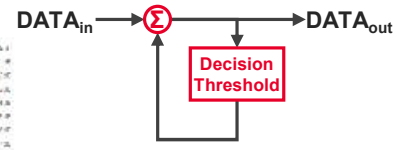


DPRX

CTLE, 10 DC gain levels

DFE





General Introduction to DisplayPort

DP2.1 SPECIFICATION UPDATES

- Target publication date: Q1 CY22
- New enhanced connectors
- Tethered sink with enhanced fsDP/mDP plug
- Cable specification is being re-written

Full-size DP	Mini DP	USB-C
		

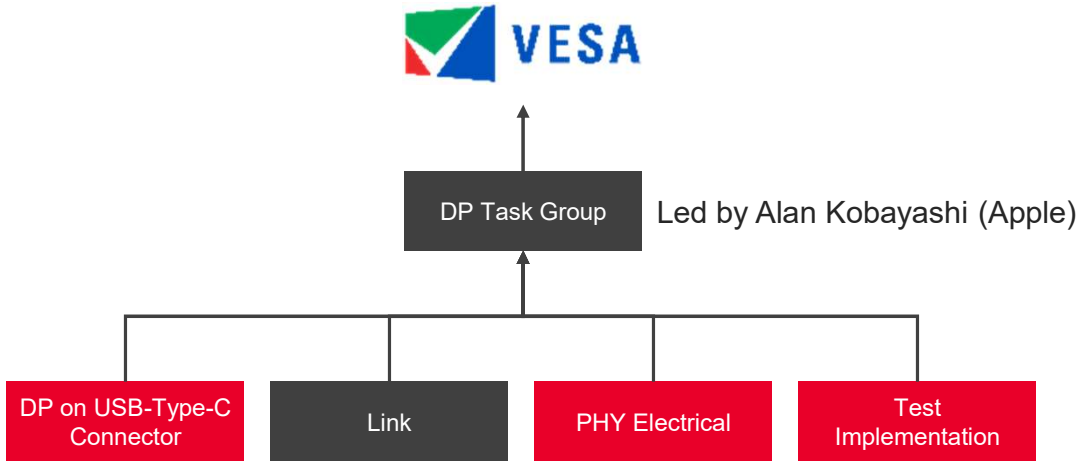
Connector	DP1.4a	UHBR10	UHBR13.5	UHBR20
fsDP	✓			
mDP	✓			
Enh fsDP	✓	✓		
Enh mDP	✓	✓	✓	✓
USB-C	✓	✓	✓	✓

Standard Committee and Compliance

Standard Committee and Compliance

STANDARD COMMITTEE

- Video Electronics Standards Association
- ~300 corporate members
- Weekly calls
  - Specification and CTS review
  - New developments
  - SCRs, ECNs…
- Not only DisplayPort
  - DisplayPort HDR
  - DisplayPort Compression Codecs
  - DisplayPort Mounting



Standard Committee and Compliance

COMPLIANCE PROGRAM

- Managed by VESA
  - Jim Choate(former Agilent USB Pyramid Lead)
- Why do companies need the logo?
  - Ensure interoperability
  - Consumers can easily identify compliant products
- How to get it?
  - Pass the Compliance Program
  - Be a member of VESA
  - Sign the VESA DisplayPort Trademark License Agreement
- Authorized Test Centers(ATCs)
  - Allion, GRL, TTA, UL..

Standard Committee and Compliance

COMPLIANCE TEST SPECIFICATION

- **DP1.4a PHY CTS rev1.0** released in July 2018
  - **DP1.4a PHY CTS rev1.1** released in June 2020
- Several DUT types
  - **Source**
  - **Sink (un)tethered**
  - Passive cables
  - Others..
- Definitions
  - Test Points
  - Test Point Access(TPA) Fixtures

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp-p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative

Item	Name	Normative/ Informative
4.1	JTOL Test	Normative

Standard Committee and Compliance

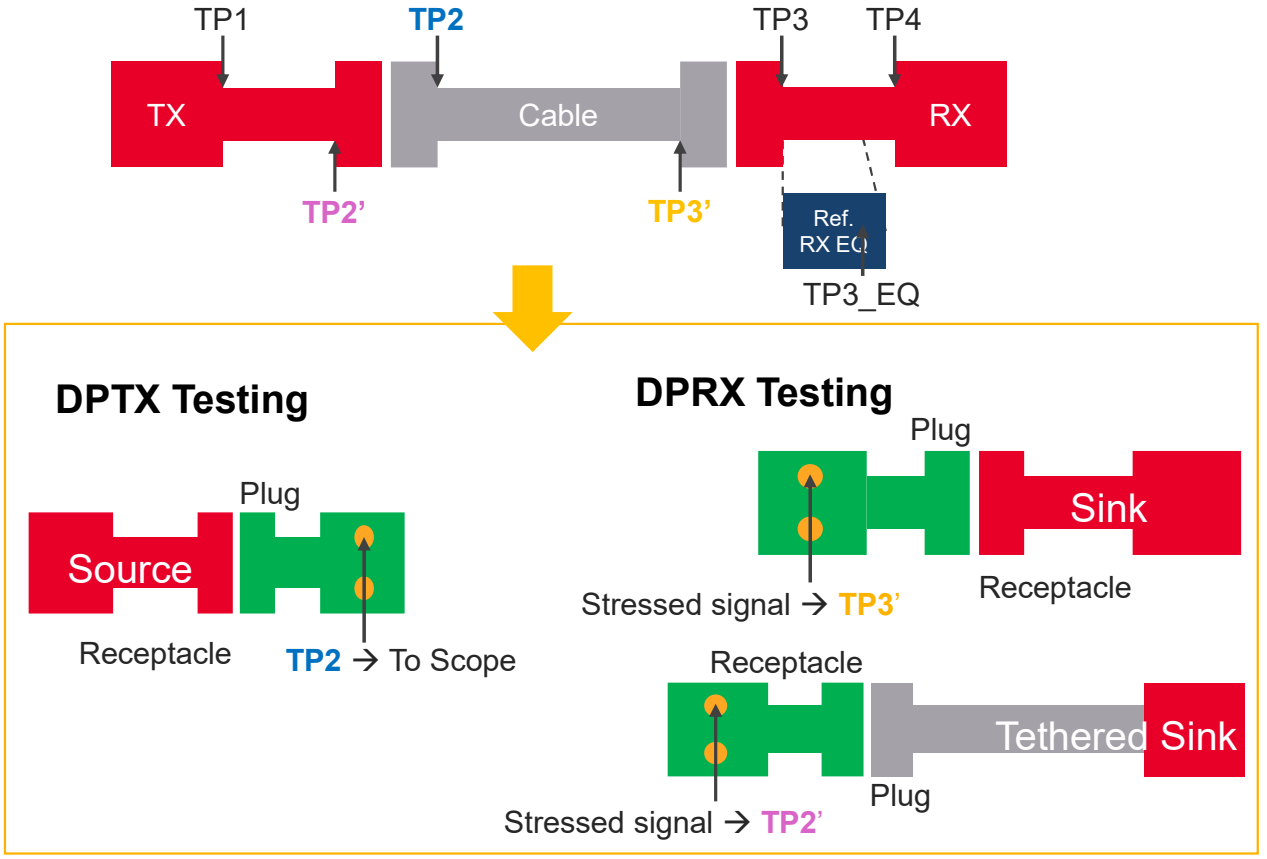
DP2.1 PHY CTS

- In progress, target publication date: Q1 2022
- Changes and additions from DP1.4a PHY CTS rev1.1
  - DP 128b/132b Source Tests
  - DP 128b/132b Sink Tests
  - AUX channel slew rate becomes informative
- Include considerations from the enhanced DP work and SCRs to the DP2.0 specification
- Offline test equipment correlation activities

Standard Committee and Compliance

TEST POINTS AND TPA EXAMPLES

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2'	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3'	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined cable model with equalization applied.'
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.



Standard Committee and Compliance

HOW TO TEST THE PHY LAYER?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

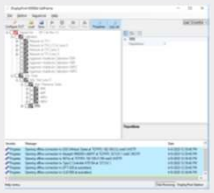
Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

Test Solutions

Keysight DisplayPort Solutions

SOURCE AND SINK TEST SOLUTIONS OVERVIEW

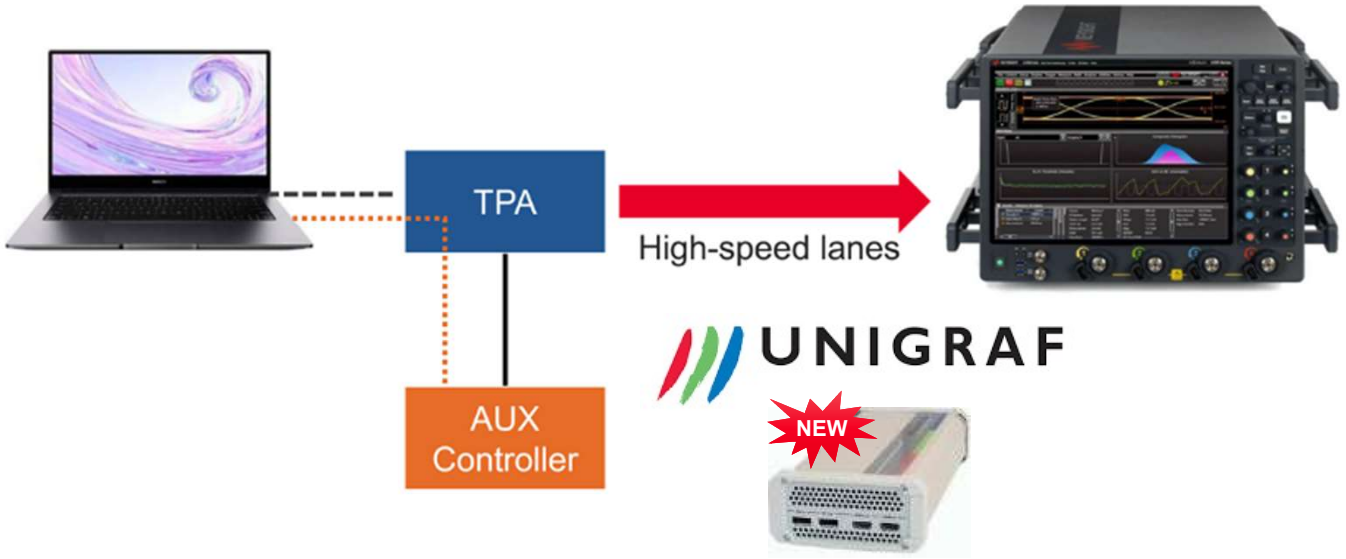
	Source	Sink
Test Automation Software	 **D9040DPPC, D9042DPPC, D9040EDPV** Automated TX tests Compliance, Debug & Characterization Automation via AUX channel	 **N5991DP2A** Accurate RX calibration Automated RX tests Compliance, Debug & Characterization Automation via AUX channel
Instruments	 **UXR** Lowest noise Fast, accurate measurements Channel embedding & de-embedding CDR, Equalization, Eye/Jitter analysis	 **M8000** Best signal integrity Lowest noise Equalization, RJ, PJ, CMI Test patterns
Accessories	 **DPR-100** Reference Sink 	**DPT-200** Reference Source 

DisplayPort Source Test Solution

HOW TO TEST THE SOURCE PHY LAYER?

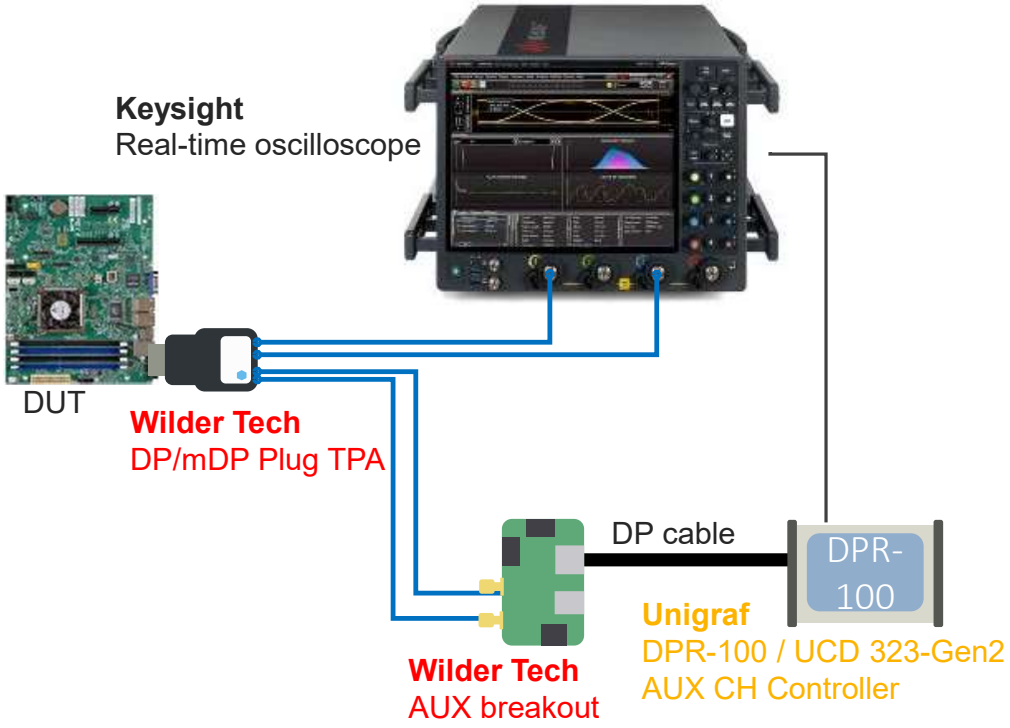
Source Overview

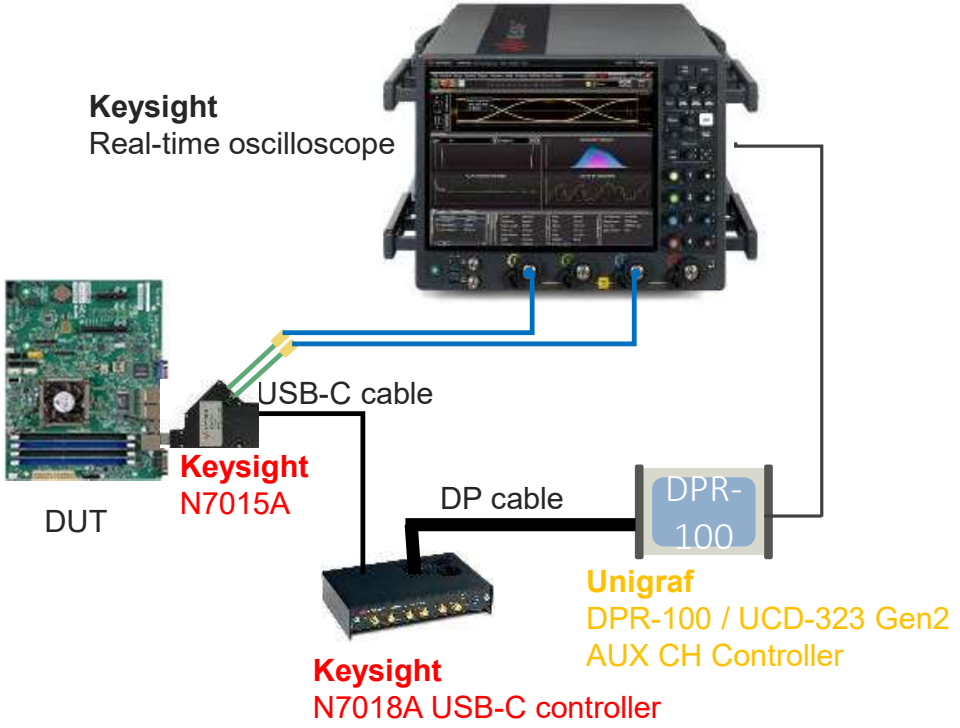
- Configure the Source to output test patterns with certain drive settings -> **AUX Controller**
- Embed worst-case channels, apply EQ on the oscilloscope
- Run measurements



DisplayPort Source Test Solution

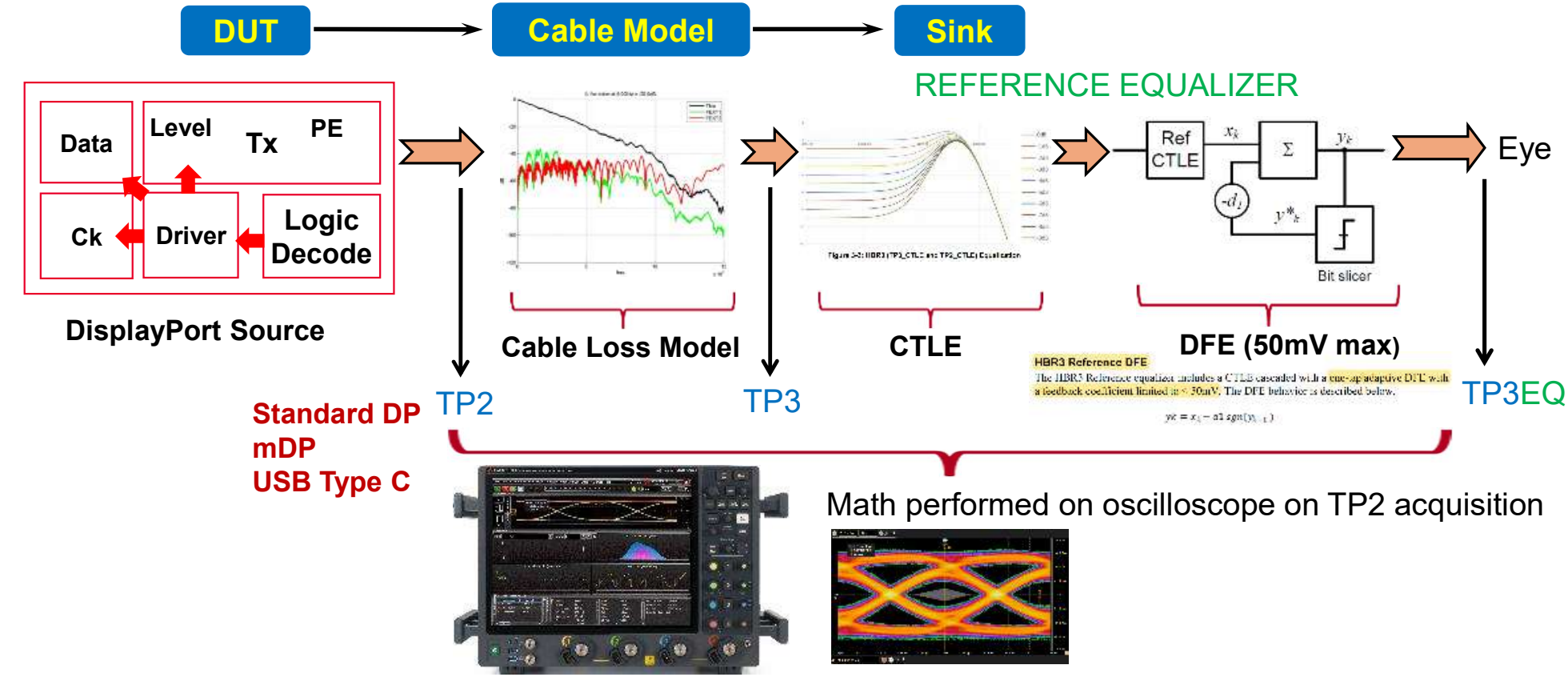
SOURCE TEST SETUP AND SOLUTIONS





DisplayPort Source Test Solution

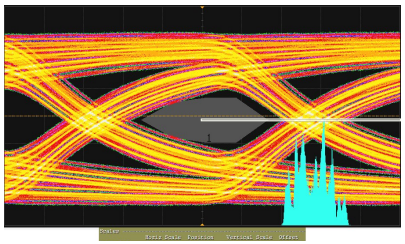
DISPLAYPORT MEASUREMENT MODEL



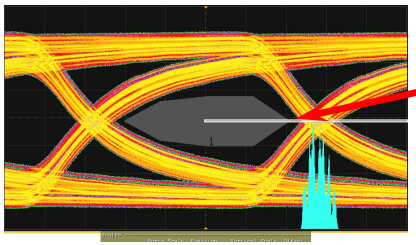
DisplayPort Source Test Solution

DISPLAYPORT EYE DIAGRAM CHANGES

- RBR and HBR



2.7 Gbs: **TP2**: PRBS7

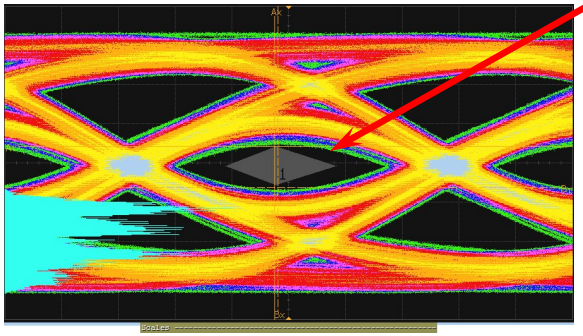


1.62 Gbs:**TP2**: PRBS7

6 Point polygon for RBR and HBR

4 Point polygon for HBR2
Vertical vertices based on widest point in the eye.

- HBR2

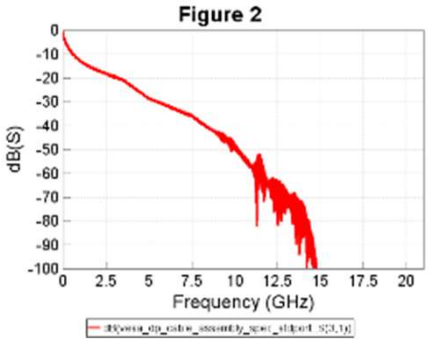


5.4 Gbs:**TP3EQ**: HBR2Compliance Pattern*

TP3EQ = TP2 Acquisition with Cable Model Embedded and Equalizer Applied. 10^{-9} BER

Cable Model

Equalizer: CTLE
DC Gain=1
Zero at 540MHz
Pole1=2.7GHz
Pole2=4.5GHz
Pole3=13 GHz
DUT state is user selectable



DisplayPort Source Test Solution

DISPLAYPORT EYE DIAGRAM CHANGES: HBR3

- Tx HBR3 Discovery of the Optimized CTLE and meeting new Eye-Hight and Jitter requirements

HBR3 TP3_CTLE Waveform EYE Height (EH): **≥65mV_diff_pp**

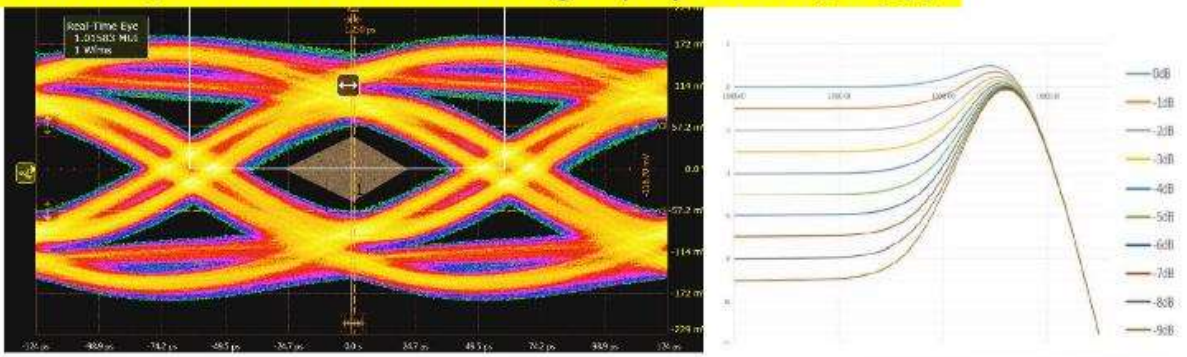


Table 3-3 defines the measurement mandates.

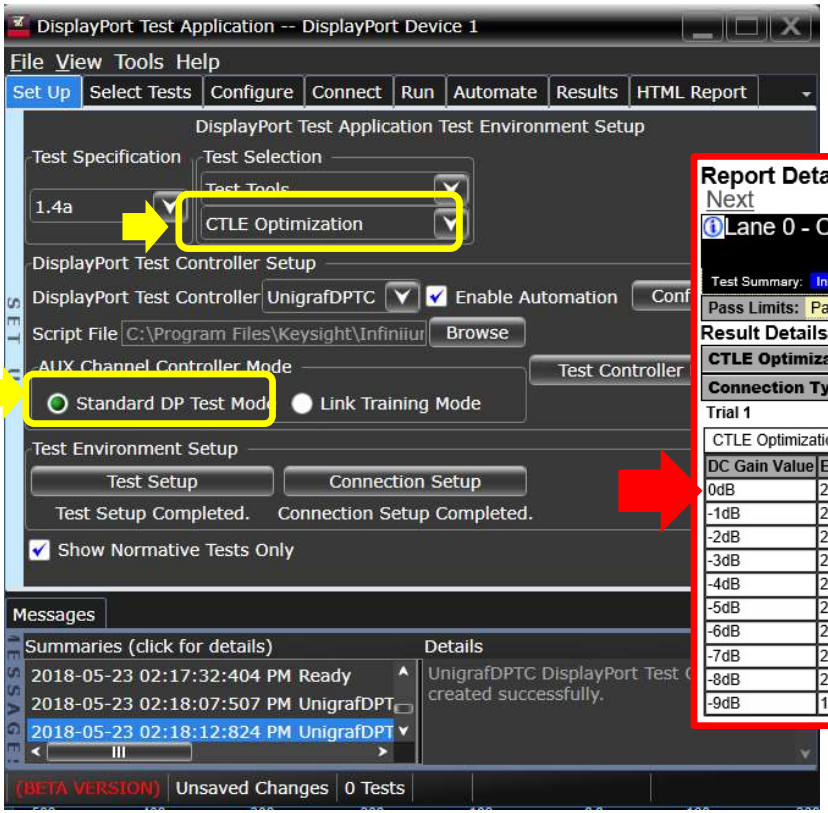
Table 3-3: EYE Diagram Test Measurement Mandates

Condition		Specification
EYE Diagram		• Shall be displayed so that more than one complete UI is shown, but no more than 2.5UI
Clock Recovery		• Shall be as defined in Section 2.1
Minimum Acquisition Time		• Shall be at least 2MUI
Equalization	**HBR3 (TP3_CTLE[a] and TP2_CTLE)**	• For each acquisition, using the appropriate cable model from Table 3-2, the analyzer software sweeps the range of CTLE Transfer Functions as defined in Table 3-4, and then uses the value with the optimal EYE Height (TP3_CTLE_Optimal) for the compliance test result (see Figure 3-5) $H(s) = A_{ac} \times \omega_{p2} \times \frac{(s + (A_{dc} / A_{ac}) \times \omega_{p1})}{(s + \omega_{p1}) \times (s + \omega_{p2})}$ where: • A_{ac} is 3.5dB • A_{dc} is an integer within the range of 0 through -8dB, inclusive, in 1-db steps • ω_{p1} = 3.03GHz • ω_{p2} = 5.60GHz • Test equipment analyzer software shall store each TP3_CTLE waveform and associated recovered clock waveform to be used in TP3_DFE compliance test evaluation, if needed
	HBR3 (TP3_DFE)[a]	• If the CTLE sweep does **not** result in a passing TP3_CTLE_Optimal result, the test equipment analyzer software shall use the VESA DFE Tool to calculate the TP3_DFE_Optimal result
	HBR2/HBR	• For each cable model acquisition listed above, the analyzer software applies a CTLE Transfer Function, as defined in *DP Standard*, *Figure 3-37* and *Figure 3-38*, for HBR2 and HBR, respectively
	RBR	• N/A

a. See Figure 3-2.

DisplayPort Source Test Solution

CTLE OPTIMIZATION FOR HBR3



Report Detail

Next

Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) - HBR2CPA

Test Summary: Info | Test Description: To find the optimized DC gain value for the CTLE.

Pass Limits: Pass/Fail | Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) - HBR2CPAT | -4dB

Result Details

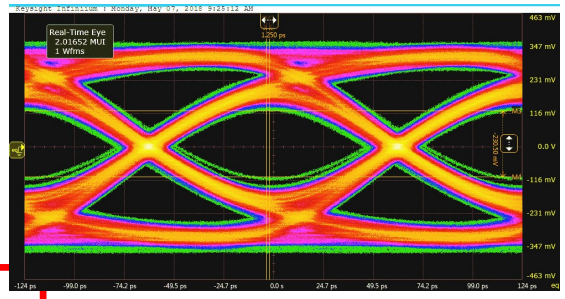
CTLE Optimization Result	(See table)	**Cable Model**	None	**Test Mode**	Compliance	**Test Sele**	
Connection Type	Single-Ended (A-B)	**BitRate**	8.1 Gbps	**SSC**	SSC Enabled	**Level**	Swing 2	**Pre**

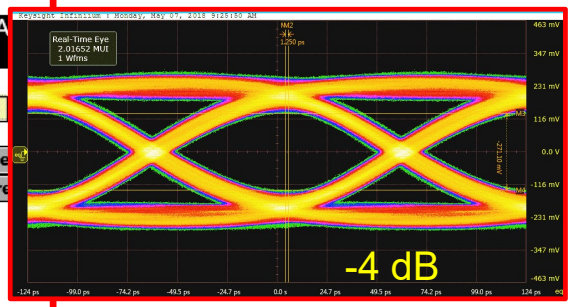
Trial 1

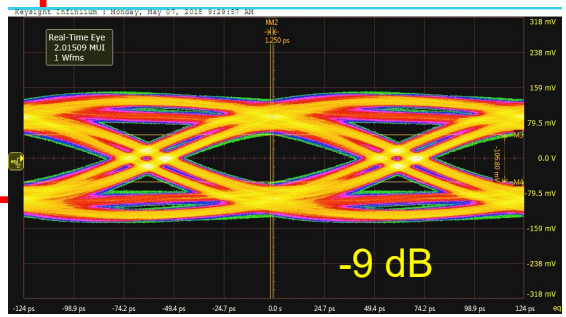
CTLE Optimization Result

DC Gain Value	Eye Height (V)	Eye Height Location (UI)	Eye Width (s)	Clock Recovery Status
0dB	230.5 m	490.0 m	91.61 p	Fully Recovered
-1dB	245.8 m	490.0 m	96.64 p	Fully Recovered
-2dB	261.2 m	520.0 m	101.3 p	Fully Recovered
-3dB	268.4 m	520.0 m	98.58 p	Fully Recovered
-4dB	271.1 m	540.0 m	97.99 p	Fully Recovered
-5dB	267.5 m	540.0 m	96.64 p	Fully Recovered
-6dB	254.9 m	490.0 m	93.74 p	Fully Recovered
-7dB	234.0 m	460.0 m	91.42 p	Fully Recovered
-8dB	213.3 m	430.0 m	89.11 p	Fully Recovered
-9dB	193.5 m	400.0 m	86.01 p	Fully Recovered

0dB



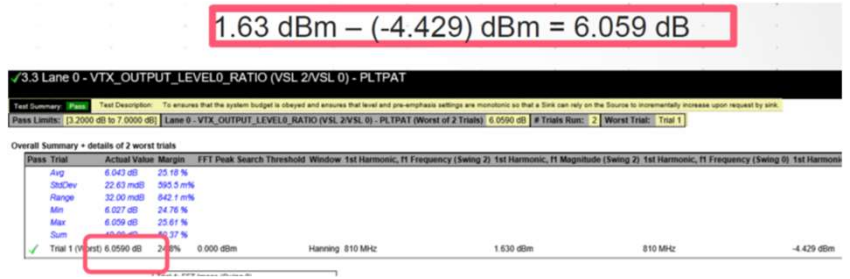


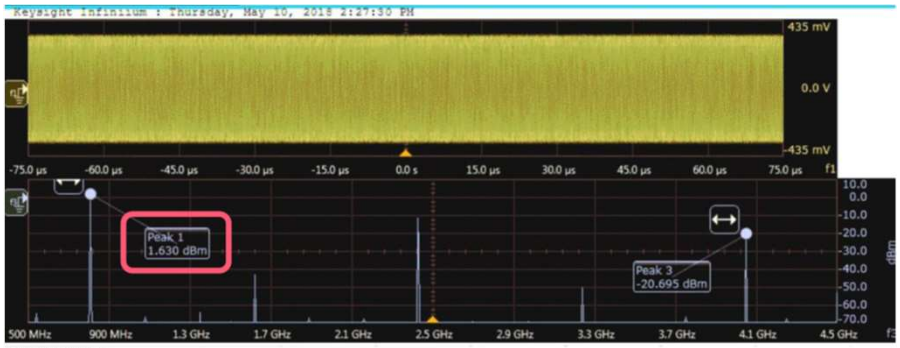


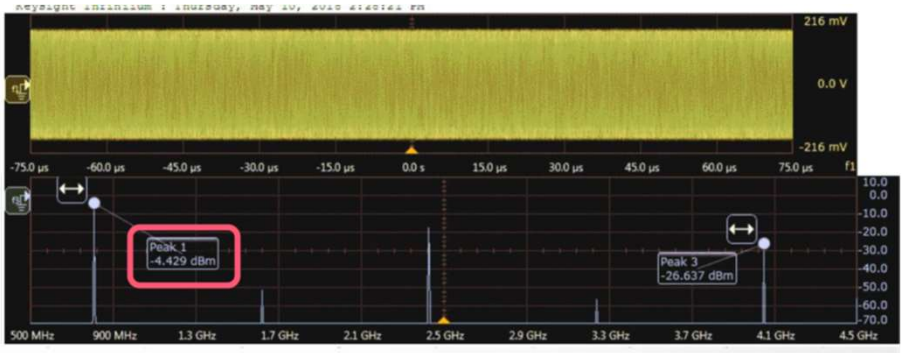
DisplayPort Source Test Solution

VLS AND PE LEVEL CHECKS: SPECTRAL METHOD

- PHY CTS 1.2b used time domain measurements to verify proper ratio changes for VLS/PE setting changes
- Accuracy and test time was always a problem
- Spectral method analyzes frequency content(harmonic amplitudes) to verify changes to VLS/PE are monotonic and meet DP 1.4a specification requirements.



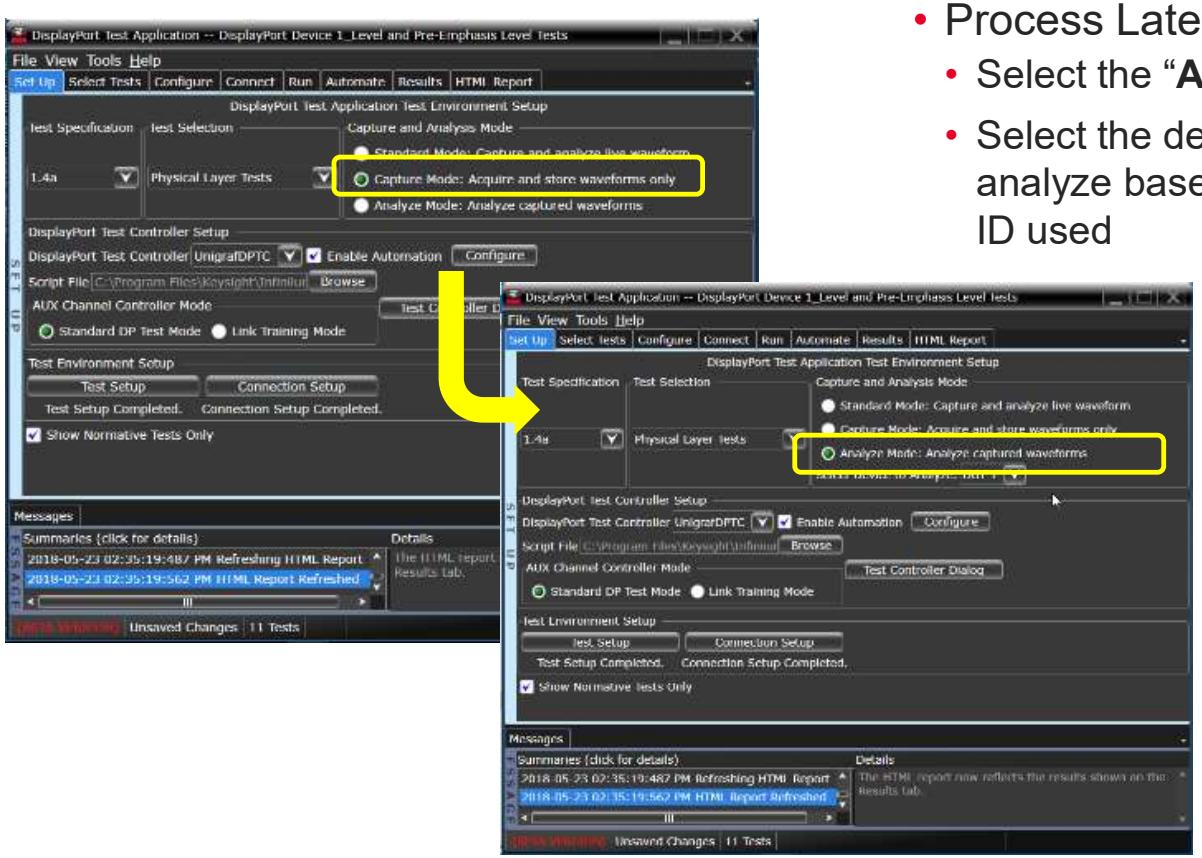




DisplayPort Source Test Solution

ACQUIRE NOW AND PROCESS LATER(ANPL)

- Acquire Now:
  - Set to “**Capture Mode**”
  - Name the “Device ID” which will be used as the Device Name of the Analysis Mode

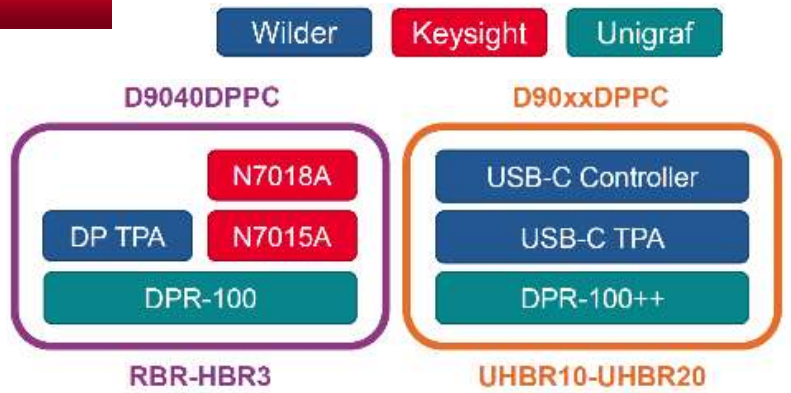


- Process Later
  - Select the “**Analyze Mode**”
  - Select the device to be analyze based on the Device ID used

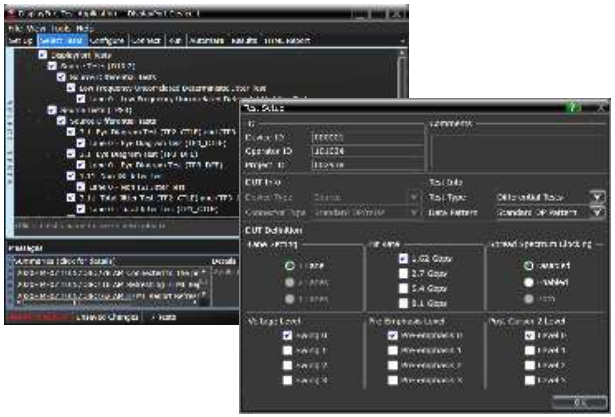
DP Source Compliance Test

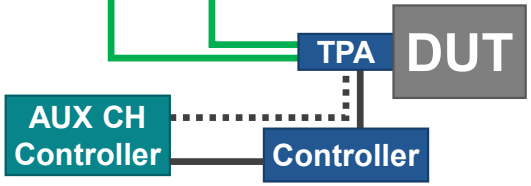
TX APPLICATION OVERVIEW

- Updated SW package **D9040DPPC**
- New SW package **D9042DPPC**
- Productivity improvements
  - ANPL(Acquire Now and Process Latter)
  - Disaggregation



D9040DPPC





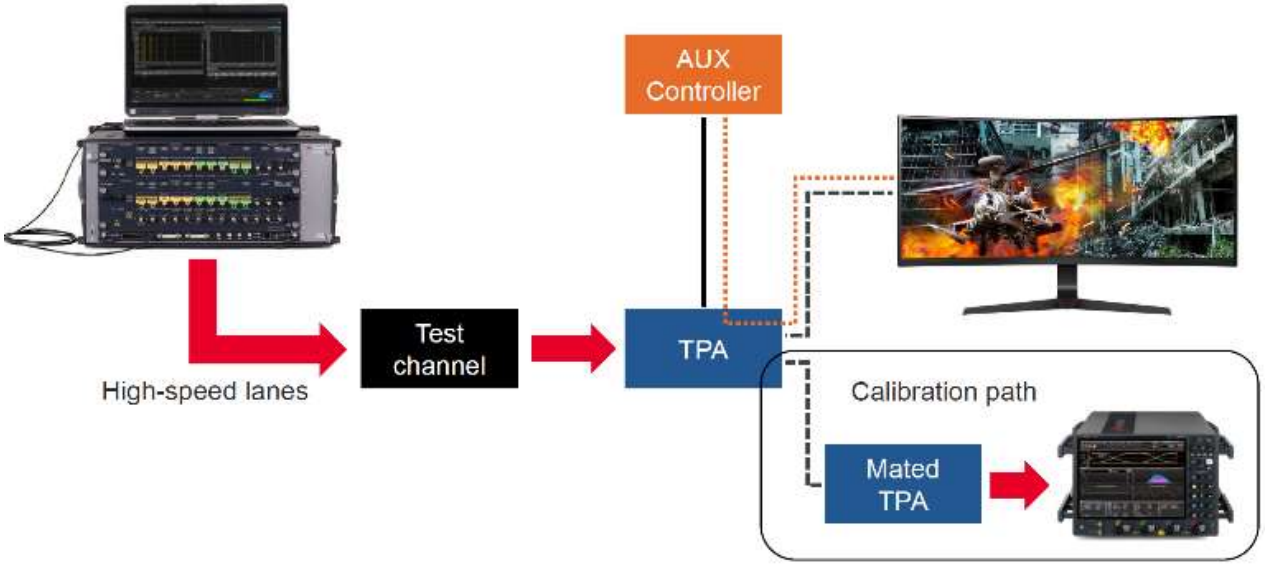
D9042DPPC

DisplayPort Sink Test Solution

HOW TO TEST THE SINK PHY LAYER?

Sink Overview

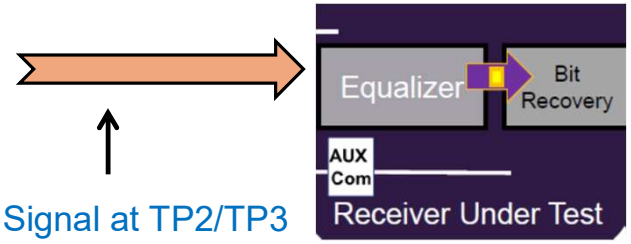
- Generate the stress signal with a pattern generator
- Guide the Sink through Link Training -> **AUX Controller**
- Read built-in error counter



DisplayPort Sink Test Solution

DP SINK JITTER TOLERANCE TEST

- Sink Jitter Tolerance which provides a stressed signal of known pattern to the DUT and the DUT measures the number of bit errors. Sink Jitter Tolerance is performed ONE LANE at a time.



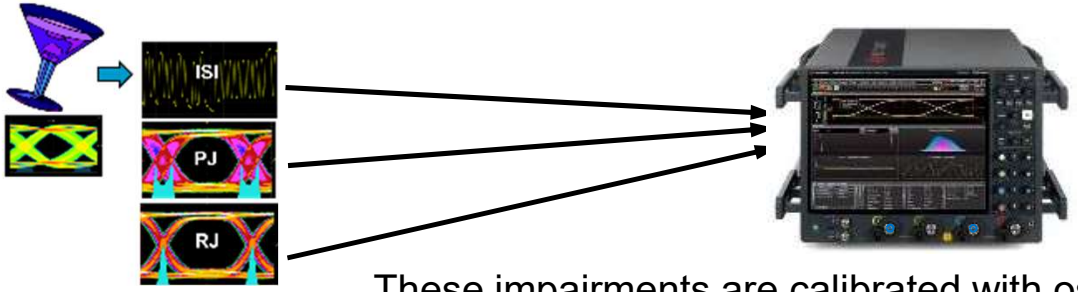
Inject Signal at TP2/TP3

TP2 / TP3

TP2

- The Stressed Signal:
  - A maximum Eye Height is specified
  - A maximum Eye Width is specified

Must apply realistic signal at TP2/TP3→ it must have precisely known 'impairments'



These impairments are calibrated with oscilloscope measurements

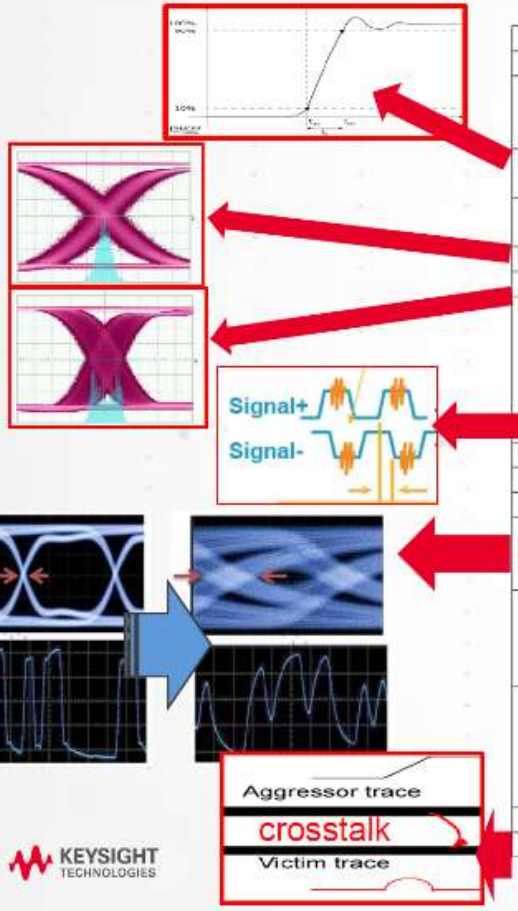
DisplayPort Sink Test Solution

KEYSIGHT MOI

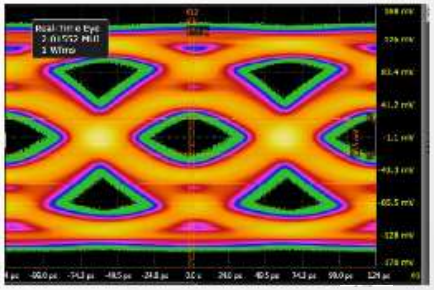
Draft version 1.0
May 10th, 2018

Keysight Draft MOI for DisplayPort™ PHY CTS 1.4 Sink Calibration and Testing Using J-BERT M8020A/N4903B and DSA90000A/X/Q/Z/V Series Oscilloscopes

DisplayPort

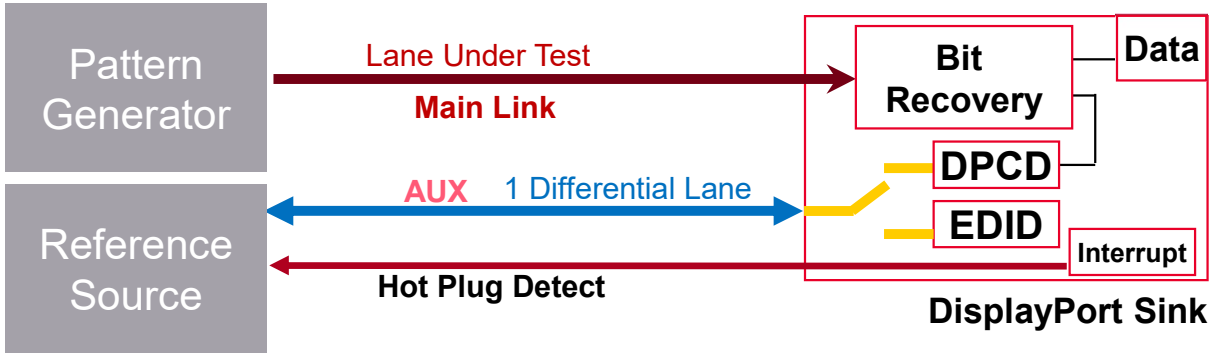


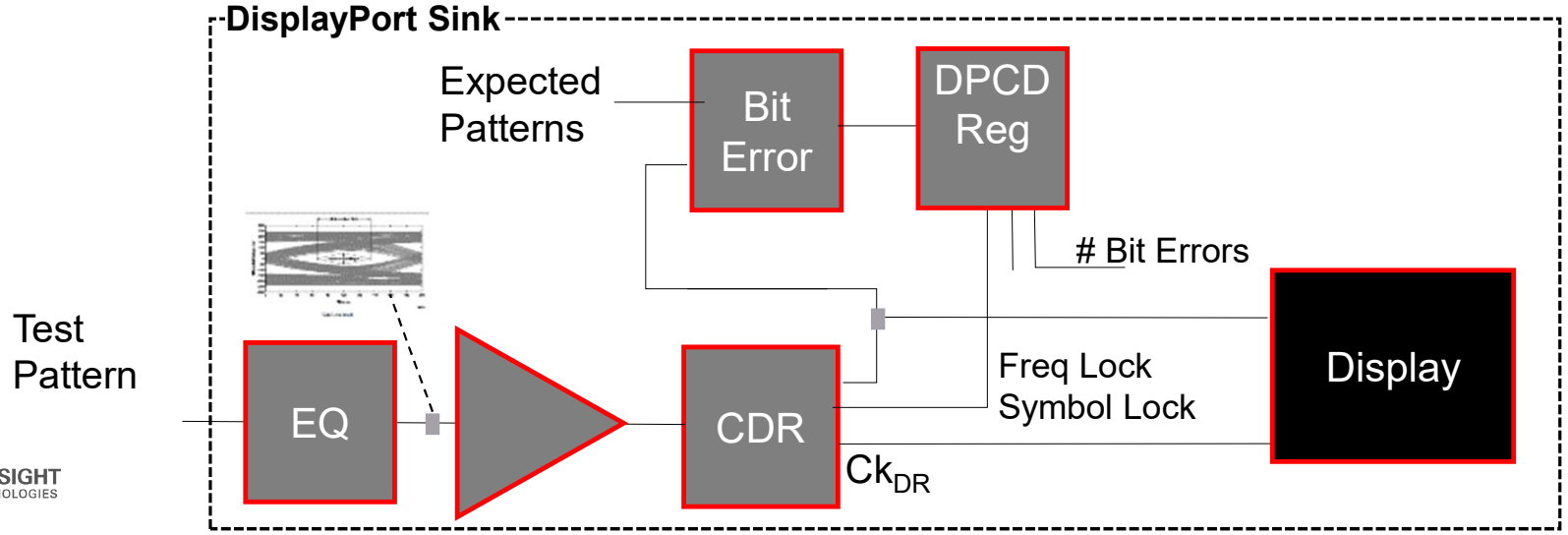
Stressed Eye Parameter	HBR3		
Bit Rate	8.1 Gb/s		
Transition Time Converter (TTC) Value for Main Link Stressed Signal	The value of the transition time converter depends on the cable + TTC combination required compliance number.		
Transition time for victim signals, measured at TP1	40 ~ 60ps (20% to 80%)		
Test Signal Pattern	TPS4 (CP2520 Pattern 3)		
RJ_{RMS}	13 mUI +/-5%		
SJ_{FIXED} @ 297MHz	130 mUI +/-5%		
SJ_{SWEEP} Approximate 2MHz 10MHz 20MHz 100MHz	 1013 mUI +/-5% 137 mUI +/-5% 109 mUI +/-5% 100 mUI +/-5%		
Common Mode Noise	100mV(p-p)@ 400MHz		
SSC	33 KHz, triangular shaped, 5000 ppm down spread		
Test Point	TP1 (Informative)	TP2 CTLE	TP3 CTLE
CTLE dc Gain	No	-4dB	-8dB
Compliance Interconnect Channel (CIC) ISI	50 mUI +/-10%	120mUI +/-5%	240mUI +0%/-5% & Loss within -22~-24dB
TJ (1E-6) [a] (after CDR) with all the impairments except Crosstalk, Crosstalk jitter of 20mUI is assumed	410 mUI +0%/-10 %	480 mUI +0%-5% (460mUI before)	600 mUI +0%/-5%
Calibrated Eye Height with all the impairments except Crosstalk (2M UIs) (49%~51% of UI), Crosstalk noise of 10mV is assumed	600 mV_{diff} +/-5%(280mV)	250 mV_{diff} +/-5%(For tethered, need to test additional EH= 170mV_{diff})	50 mV_{diff} +/-5%
Crosstalk Pattern	D24.3 i.e. the quarter rate clock pattern, TPS4 is optional choice		
Crosstalk Amplitude	300 mV_{diff}/150ps TTC		



DisplayPort Sink Test Solution

SINK TEST SETUP AND SOLUTIONS





DP Sink Compliance Test

RX APPLICATION OVERVIEW

- New SW package **N5991DP2A**
- Automated Sink calibration and tests
- All PHY rates **from RBR to UHBR20**
- Standard DP and USB type-C connector

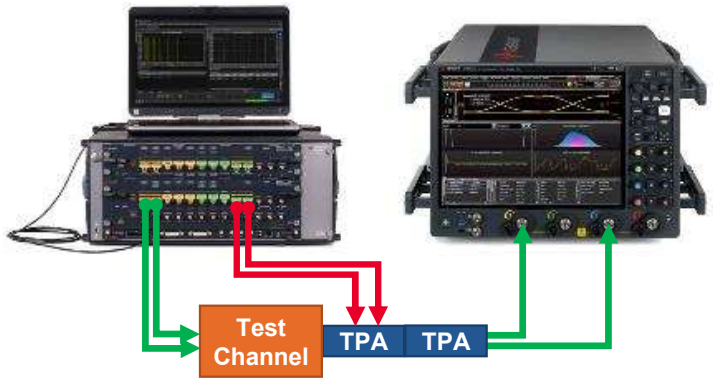
Wilder | Keysight | Unigraf

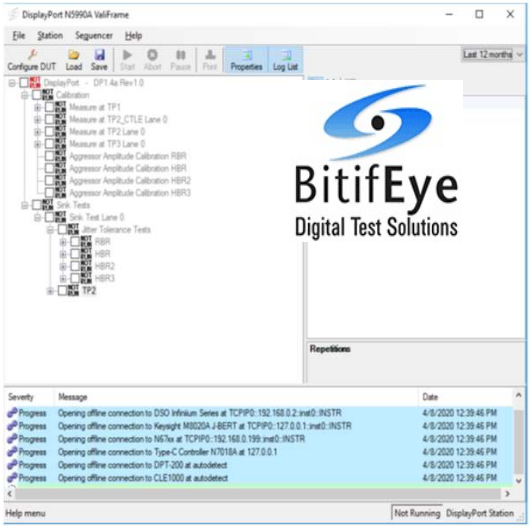
N5991DP2A

	N7018A	USB-C Controller
DP TPA	N7015A	USB-C TPA
DPT-200		DPR-100++

RBR – UHBR20

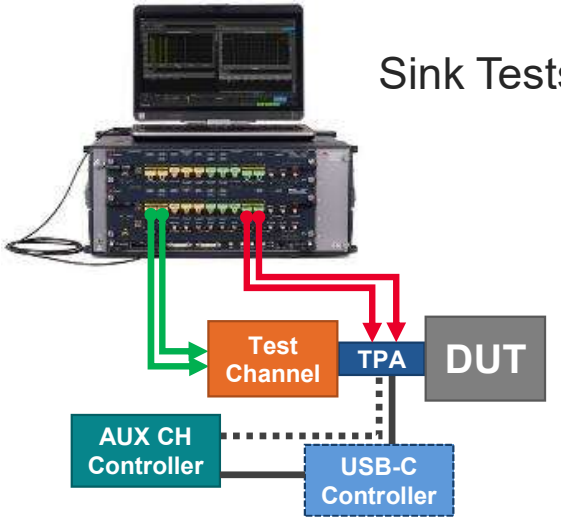
Calibrations





DisplayPort Physical Layer Testing

Sink Tests



Part 2 Agenda：HDMI

- Background and Introduction
  - HDMI Overview
  - HDMI Technology
- Keysight HDMI Test Solutions
  - HDMI Solutions Overview
  - HDMI Source Test Solution
  - HDMI Sink Test Solution
  - HDMI Active Optical Cable Test Solution
  - HDMI eARC Test Solution

Background and Introduction

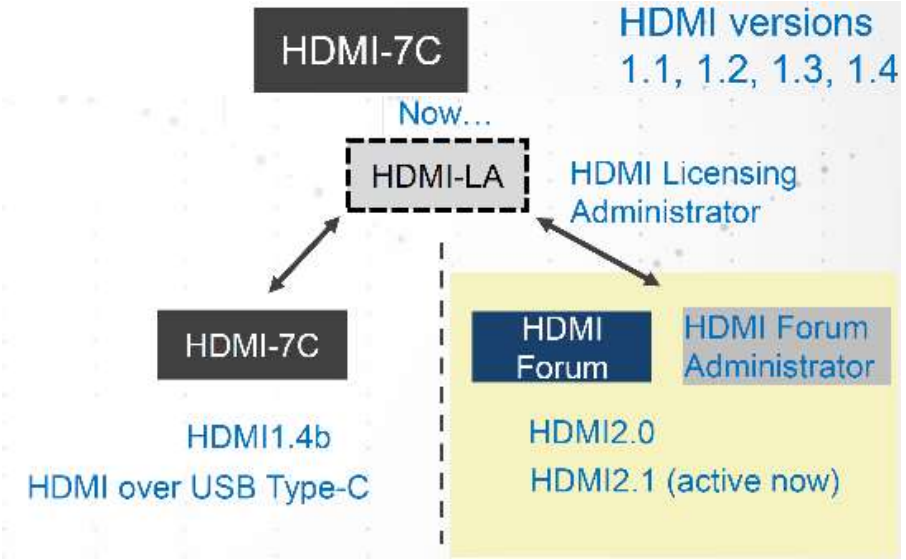
HDMI Overview

ORGANIZATION

- HDMI owned by the 7C

(Thompson, Hitachi, Silicon Image, Panasonic, Philips, Toshiba, Sony)

- In 2011 the HDMI Forum was created
  - Charter: responsible for future of HDMI for rates > 3.4Gbs per lane
  - HDMI 7C owns HDMI1.4 LA is formed
- 2013 HDMI Forum Rolls out HDMI 2.0
- 2017 HDMI Forum introduces HDMI2.1 Specification



HDMI2.1 products inherit HDMI1.4b functionality. HDMI over USB Type-C is NOT of HDMI 2.x functionality

HDMI Overview

THE STANDARDS

HDMI Founders — Thompson, Hitachi, Silicon Image, Panasonic, Philips, Toshiba, Sony

HDMI Licensing Authority (HDMI LA)

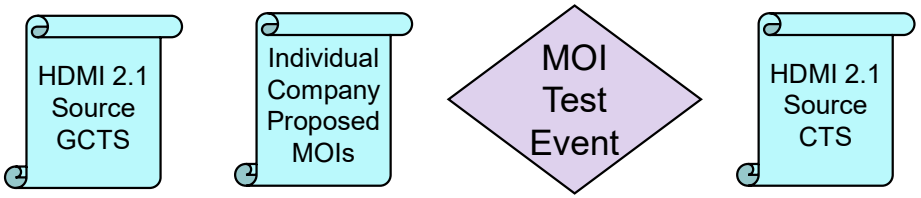
HDMI FORUM

George Burgess
ATC oversight — Verification Coordinator

Hdmi ATCs

- Marketing Working Group — Future of HDMI
- Technical Working Group — HDMI 2.x spec
- F2F meetings
- Phy SubGroup
- Test SubGroup — GCTS, CTS & MOIS docs
- MOI Test events

GCTS2.1 Top Doc
Sources GCTS2.1
Sinks GCTS2.1
Repeaters GCTS2.1
Cable GCTS2.1
eARC GCTS2.1
Connectors GCTS2.1
CEC GCTS2.1
Test Point Access Fixtures GCTS2.1



June 2020, Forum has launched a “Test Disciplines” Initiative.

- Source, TMDS
- Source, FRL
- Source, eARC RX
- Sink, TMDS
- Sink, FRL
- Sink, eARC TX
- Repeater, TMDS
- Repeater, FRL
- Source, Sink, and Repeater CEC 2.0
- Cables, Category 3

HDMI Overview

KEYSIGHT HDMI PHY COMPLIANCE TEST HISTORY AND TEAM

Brief History

2003: Agilent joins HDMI adopters.

2006: Agilent solution set for HDMI1.3 sweeps ATCs

2013: HDMI Forum membership and board membership

2014: HDMI 2.0 TX and RX solutions introduced. Keysight is born

2016-2019: HDMI Forum TSG Chairmanship

2018: HDMI2.1 TX Phy, eARC, RX Phy, and Cat3 cable solutions

2020: Active Optical Cable (AOC) specs and solution released.

2020: Early definition work for HDMI2.2

L-R: Brian, Zuhaib, How Yen, Kim Huay, Kenneth

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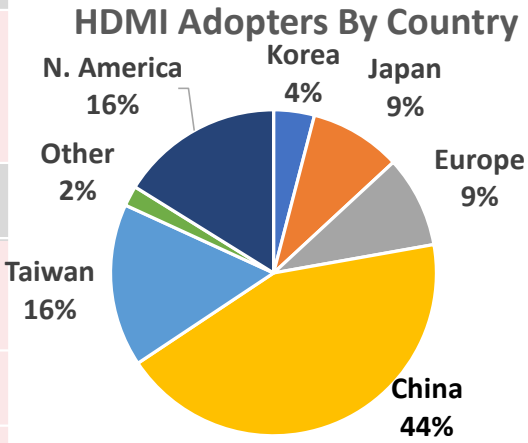
HDMI Overview

HDMI SPECS AND ADOPTERS AT A GLANCE

	HDMI Version				
	1.0–1.2a	**1.3–1.3a**	**1.4–1.4b**	**2.0–2.0b**	**2.1**
Release Date	Dec 2002 (1.0) May 2004 (1.1) Aug 2005 (1.2) Dec 2005 (1.2a)	Jun 2006 (1.3) Nov 2006 (1.3a)	Jun 2009 (1.4) Mar 2010 (1.4a) Oct 2011 (1.4b)	Sep 2013 (2.0) Apr 2015 (2.0a) Mar 2016 (2.0b)	Nov-17
Signal Specifications					
Max. Transmission Bit Rate (Gbit/s)	4.95	10.2	10.2	18	48
Max. Data Rate (Gbit/s)	3.96	8.16	8.16	14.4	42.6
Max. TMDS Character Rate (MHz)	165	340	340	600	N/A
Data Channels	3	3	3	3	4
Encoding Scheme	TMDS 8b/10b	TMDS 8b/10b	TMDS 8b/10b	TMDS 8b/10b	FRL 16b/18b
Encoding Efficiency	80%	80%	80%	80%	88.80%



HDMI Overview

KEY PLAYERS

Chip vendors

★ 

etc

★Integrators

etc

Cable Vendors

Passive
many
Active

etc

Connectors

etc

★ATCs

etc

HDMI Overview

HDMI AUTHORIZED TEST CENTERS 2019

France - Caen
- PRESTO Engineering

S. Korea - Gyeonggi-do
- *Simplay Labs (DTNC)*

Japan - Osaka
- *Panasonic Corporation*

Japan - Osaki
- *Sony HDMI ATC*

Japan - Gotanda
- *Sony HDMI ATC*

China - Shanghai
- **Philips HDMI ATC - Granite River Labs**
- **Simplay Labs**
- *Sony HDMI ATC (Allion)*

USA - Santa Clara*
- *Simplay Labs, LLC.*

Taiwan – Taipei
- *Philips HDMI ATC - Granite River Labs*
- *Sony HDMI ATC (Allion)*
- iST* (TBC)

Taiwan – Hsinchu
- **Simplay Labs (iST)**

China - Beijing
- **Simplay Labs (CESI)**

China - Shenzhen
- **Simplay Labs**
- **Sony HDMI ATC (Allion)****
- **Technicolor Trademark Management SAS - Aplus Labs**

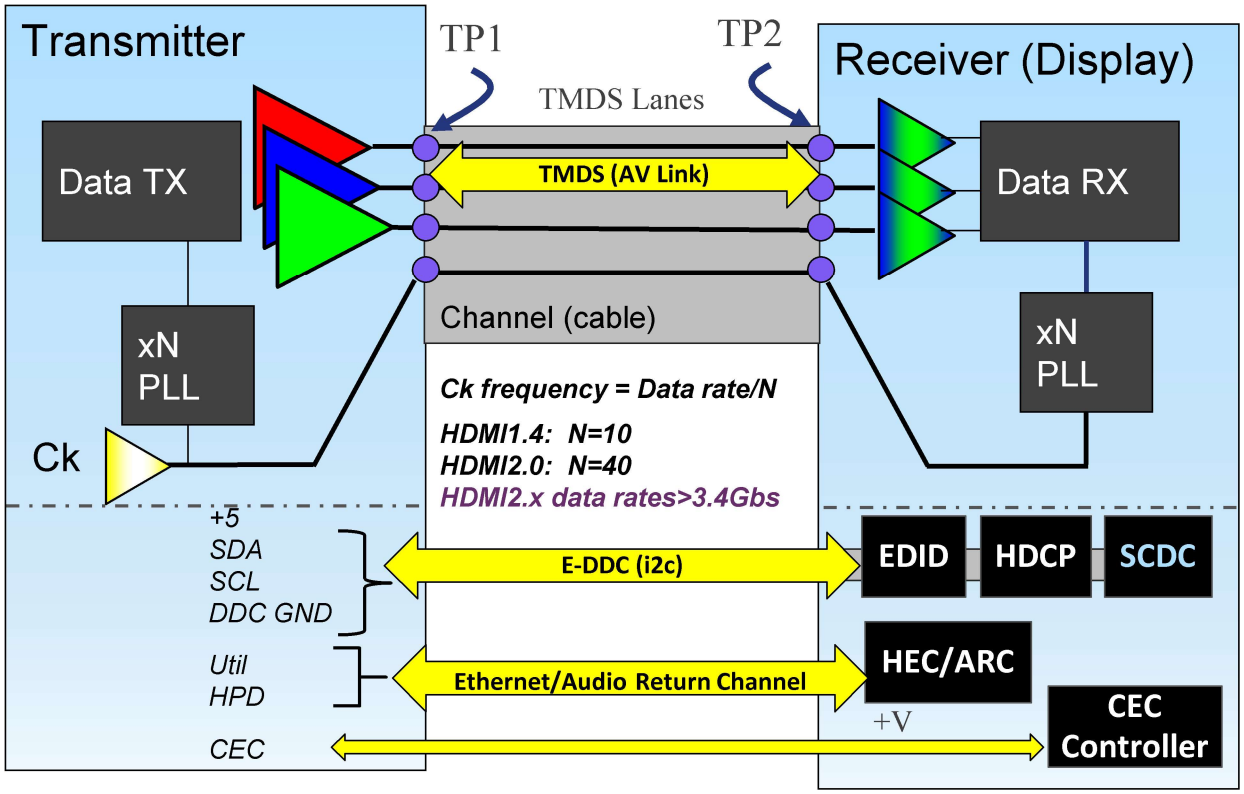
China - Dongguan City
- **Philips HDMI ATC - Granite River Labs**

LEGEND:
Keysight HDMI2.1 customer
Keysight HDMI2.0 customer
Tektronix HDMI2.1 customer
Tektronix HDMI2.0 customer
ATC but no HDMI2.1 test equipment
Highlighted = HDMI2.1 opportunity

HDMI Technology

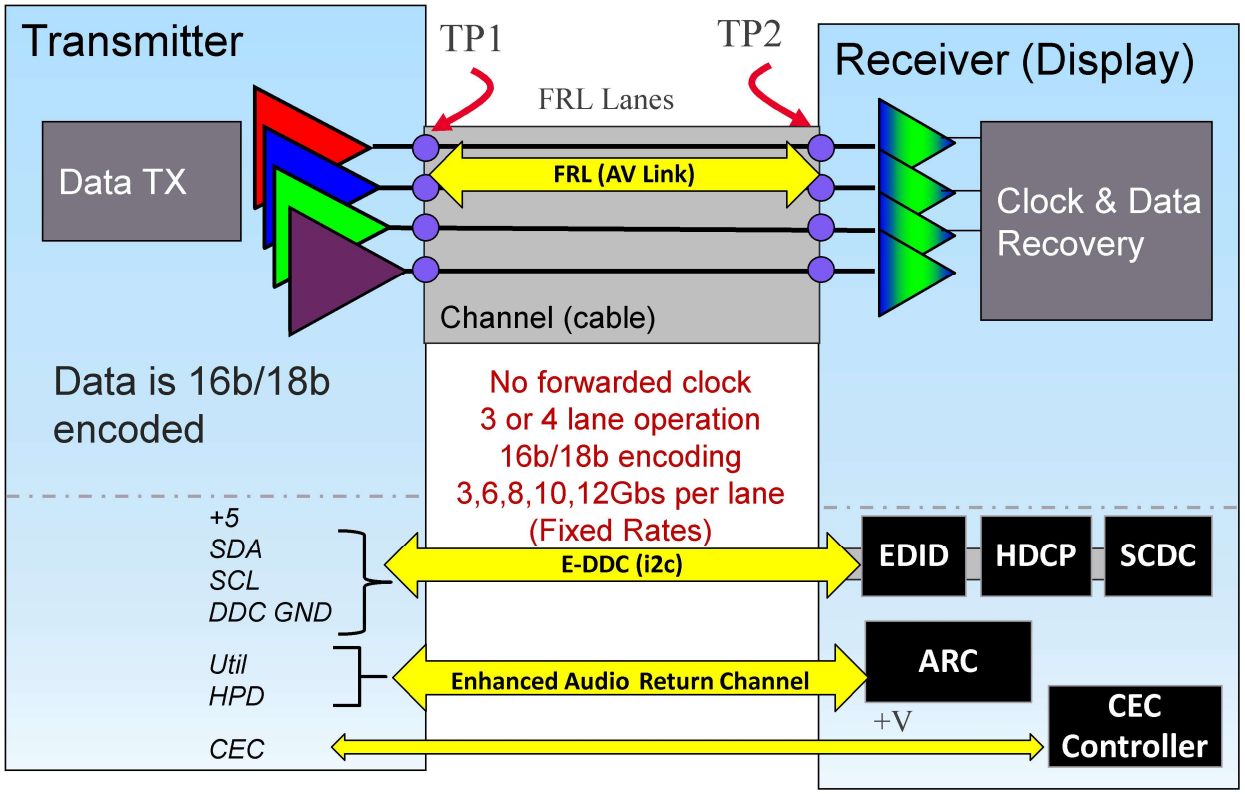
HDMI 1.4/2.1 TMDS: INTERFACE

Data is 8b/10b encoded for 1.4
Is scrambled for HDMI 2.1 TMDS



HDMI Technology

HDMI 2.1 FRL: INTERFACE



HDMI2.1 Max Payload:12Gbsx4x[16/18]= 42.67Gbs

HDMI Technology

HDMI 2.0 VS HDMI 2.1 TESTING

Specification Ver	HDMI 1.4	HDMI2.0	HDMI 2.1
Explicit Clock Lane	Yes	Yes	No
Connection Model	Differential and Single Ended	Single Ended	Single Ended
Eye Diagram/Jitter connection	Two scope channels (Data lane and Clock)	4 scope channels (Data lane and Clock)	2 scope channels (Data lane only)
Encoding	TMDS 8b/10b	TMDS 8b/10b	FRL 16b/18b
Bit Rate	250Mb/s to 3.4Gbs	3.4 Gb/s to 6Gbs	3 Gbs to12Gbs
Test Patterns	None	None	Yes

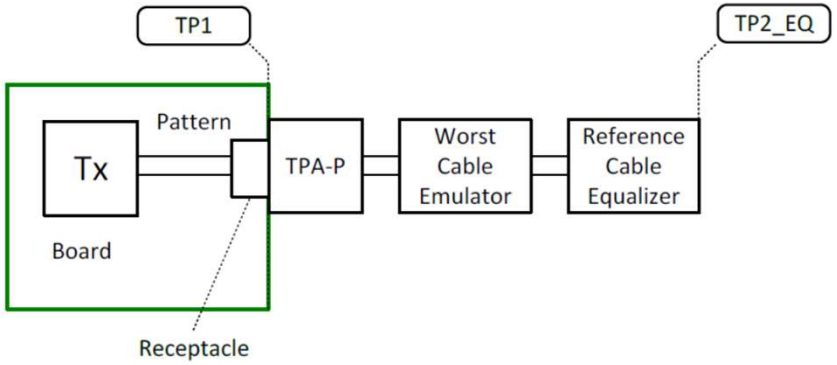
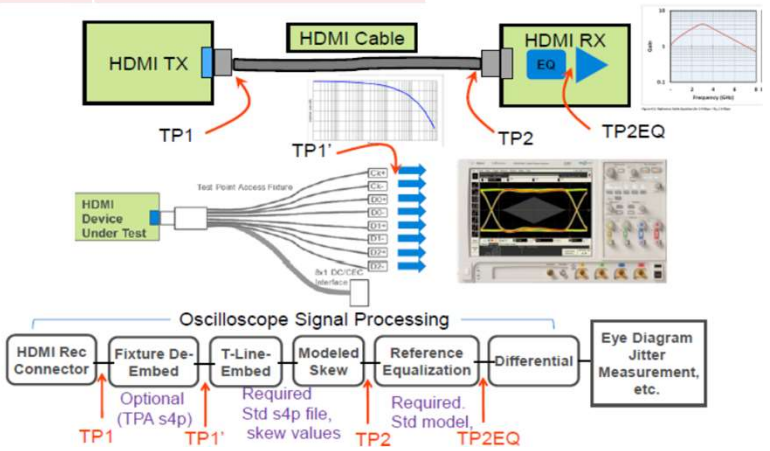


Figure 6-3: HDMI Source Test Point for Eye Diagram



Keysight HDMI Test Solutions

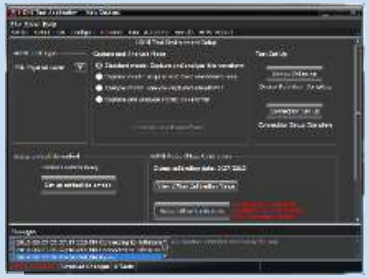
Keysight HDMI 2.1 Compliance Solutions

Source Phy Layer

N7010
N7003 + N5444A

V, Z and UXR Series Oscilloscopes

Approved MOIs



D9021HDMC Compliance Software

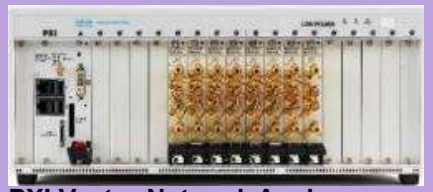
EDID/SCDC Controller

HDMI Plug TPA

Category 3 Cable and Connector Test

Setup Files

E5071C 4 port Vector Network Analyzer



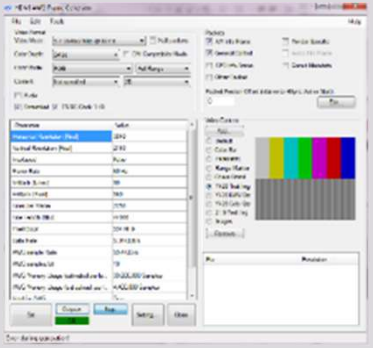
M937x PXI Vector Network Analyzer

Approved MOIs

HDMI Receptacle TPAs

Sink Phy Layer

M8195A AWG + infrastructure



Approved MOIs

N5991HP1A Compliance Software

EDID/SCDC Controller

BitifEye Digital Test Solutions

HDMI Plug TPA

Tx — Source — Cable — Sink — Rx

Keysight HDMI 2.1 Compliance Solutions

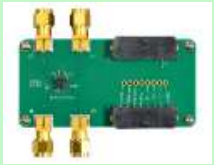
eARC Phy Layer

D9021HDMC Compliance Software

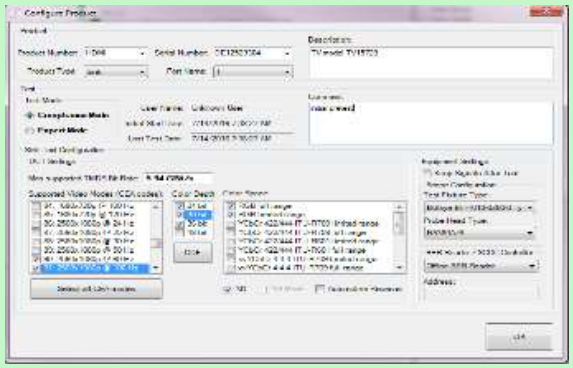
S, V, Z and UXR Series Oscilloscopes

DSGA from Bitifeye

Approved MOIs



Test Point Access Fixtures



N5991HE1A HEAC and eARC Compliance Software

81160A function generator for differential signal

Source Test

Source Phy Layer

N7010
N7003 + N5444A

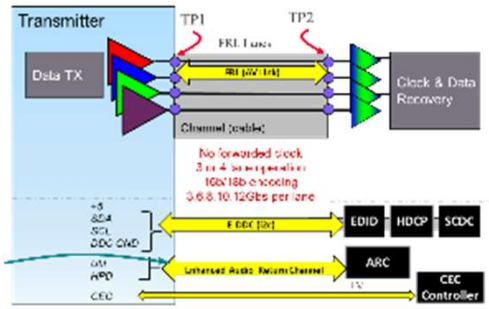
V, Z and UXR Series
Oscilloscopes

Approved
MOIs

D9021HDMC Compliance Software

HDMI Plug TPA

Keysight TX Solution



Source Phy Layer

N7010
N7003 + N5444A

V, Z and UXR Series Oscilloscopes

Approved MOIs

D9021HDMC Compliance Software

EDID/SCDC Controller

HDMI Plug TPA

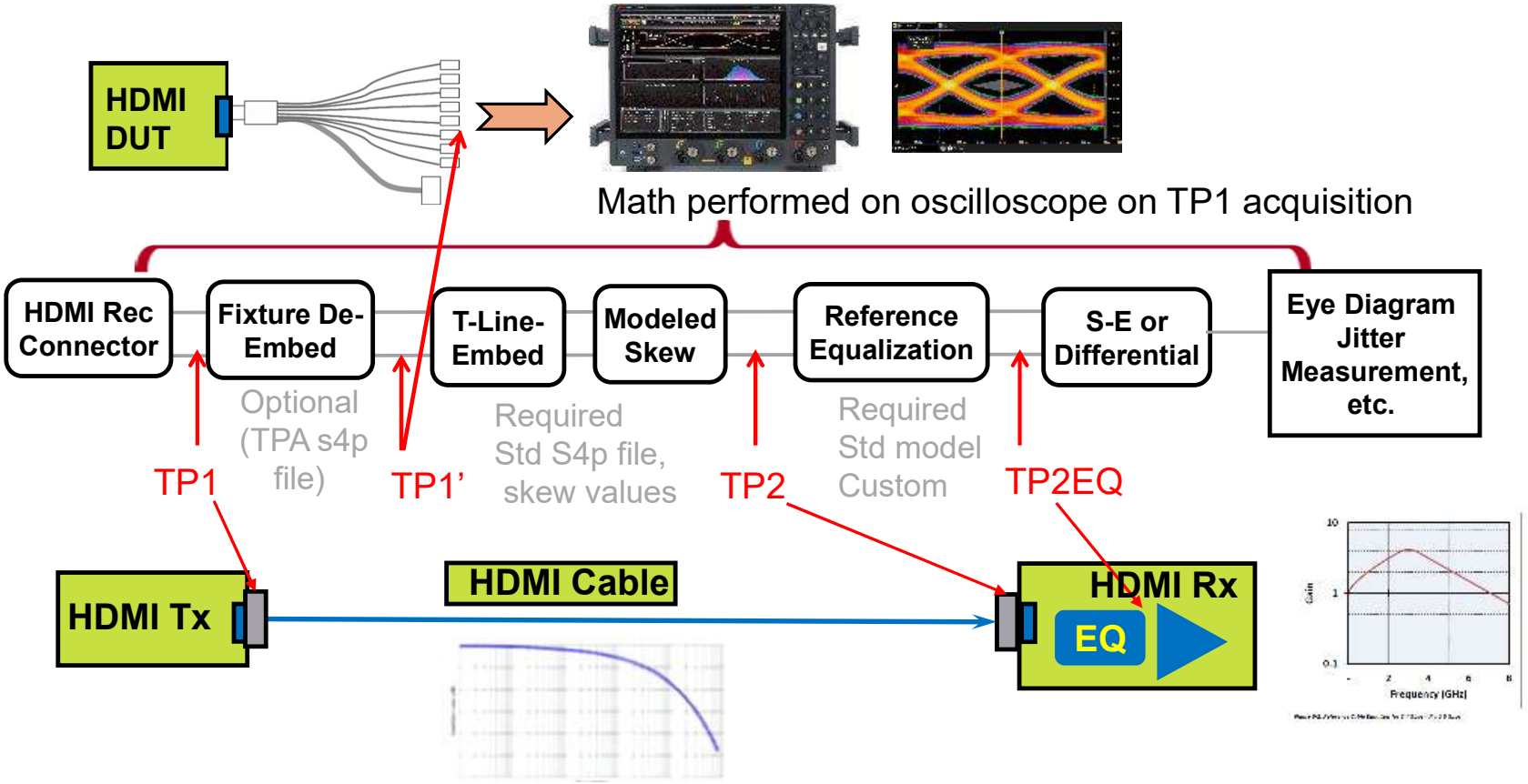
	Single Ended Connections		Differential Connections		
HDMI1.4	Single Ended Tests				
	Differential Tests				
	1169B N700xA N280xA	N5380B N5444A	1169B N700xA N280xA	N5380B N5444A	Low cost: 2 of each 4 probes makes differential go fast but SE takes extra effort.
	N7010A				Lowest cost: 4 but HDMI only
HDMI2.0	Single Ended Tests		Switch Box Automation		
	Differential Tests				
	N700xA N280xA N7010A	N5444A	Optional requires switch box and cabling (HDMI 1.4 and 2.1 TMDS)		4 each required N700xA enables ¾ full automation Switch box for full automation
HDMI2.1	Single Ended Tests				
	Differential Tests				
	N7003A N280xA N7010A	N5444A	Optional requires switch box and cabling (HDMI 1.4, 2.1)		4 each required N7003A enables full FRL automation Switch box for full automation

MX0023A + MX0105A support in progress

KEYSIGHT TECHNOLOGIES

HDMI Source Test Solution

HDMI MEASUREMENT MODEL



Source Tests

SOURCE TESTS OVERVIEW

Source Tests:

- Test ID HFR1-1: DC Common Mode
- Test ID HFR1-2: Vse_max, Vse_min
- Test ID HFR1-3: T_{RISE}, T_{FALL}
- Test ID HFR1-4: Inter-Pair Skew
- Test ID HFR1-5: TMDS/FRL Rates
- Test ID HFR1-6: Data Jitter (Rj)
- Test ID HFR1-7: Data Eye Diagram
- Test ID HFR1-8: AC Common Mode Noise
- Test ID HFR1-9: FFE

Source Tests:

- Test ID HF1-1: VL and Vswing
- Test ID HF1-2: T_{RISE}, T_{FALL}
- Test ID HF1-3: Inter-Pair Skew
- Test ID HF1-4: Intra-Pair Skew
- Test ID HF1-5: Differential Voltage
- Test ID HF1-6: Clock Duty Cycle and Clock Rate
- Test ID HF1-7: Clock Jitter
- Test ID HF1-8: Data Eye Diagram

Tests: HDMI2.1 TMDS

Test	Name	Test point	Pattern	Details
HF1-1	Vlow	TP1	Random	Vlow single ended, 3 lows in a row steady state Vbase and Vaverage of Histogram. 16M captures for all so we can use just one captured waveform for all tests.
HF1-2	Transition time	TP1	Random	Differential rise time/fall time: standard 20/80 Vbase and vtop. Vaverage for center crossing. Diff and se connections.
HF1-3	Inter pair skew	TP1	Random	Sync word available only once a frame. Full capture 200M recommended (can do 50). Special script 10MPt at time. Down to 20GSa. 1.4 the sync word is every line no problem. Retries 3 times and fail. 2 Reconnections to get full. Can use 4 diff probes for this test to get the skew job done with one connection. Can use hwst on Vseries if they have it
HF1-4	Intra pair skew	TP1	Random	Single ended connection, use average of each as the crossing point. Delta rising to falling. D+ to D-
HF1-5	Tp1 voltage swing	TP1	Random	Measure peak to peak—form eye and measure Vmax-Vmin.
HF1-6	Tmds clock Duty cycle/clock rate	TP1	Random	Scope duty cycle all edges. Picks min 49%
HF1-7	Clock jitter very different from hdmi1.4	TP2EQ	Random	We must have cable model skew left and skew right. No jitter separation so just peak to peak of histogram at center crossing. Requires single ended connection.
HF1-8	Data eye	TP2EQ	Random	Requires single ended connection for ck+, ck-, d+,d- No mask expansion, ref eq (CTLE). Infiniisim implements cable model,skew and ctle in one model. Can use transfer function section put fixture de embedding, own cable embedding and own equalizer. Length of cable equalization (2,5,7m) and can add skews to this cable equalizer

Tests: HDMI2.1 FRL

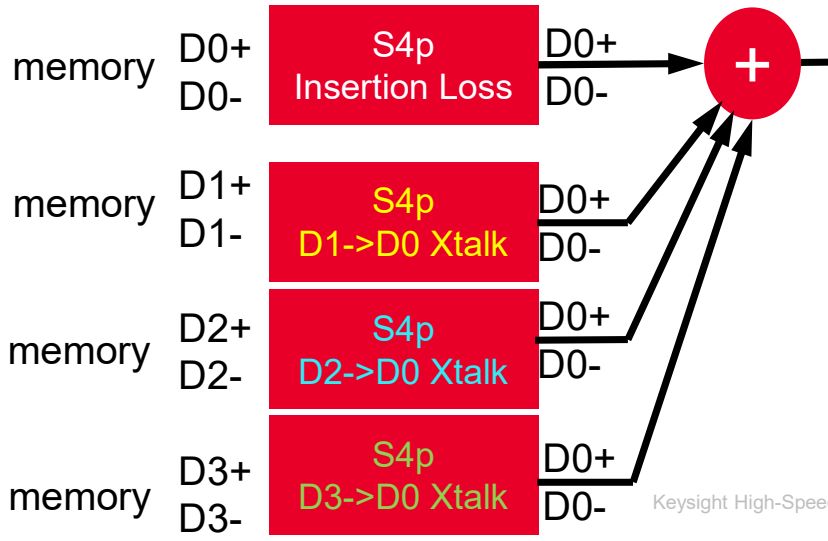
Test	Name	Test point	Pattern	Details
HFR1-1	Dc common mode	TP1	LTP5-8	Average of each L+,L- /2. If using a N5444A make sure selected properly because we do a 55 ohm correction. Common mode rejection ration offset must be done. With non- tested lanes quiet
HFR1-2	Vse Min max	TP1	LTP5-8	Vswing min to max separate limits. Single ended condition .
HFR1-3	single ended slew rate 200kpt 500 edges	TP1	LTP4	Use average as center point. 60/40 threshold for measuring slew rate. Histogram mean.
HFR1-4	Inter-pair skew	TP1	LTP5-8	Two lanes compared using SSB bit which starts the pattern for each lane. 10MPt capture that many occurrences and measure the average of the skews of these. Only se connection allowed right now. Test is tricky at 12 G. 40G sample rate, so sometimes SI sucks. Work arounds exist that you can dial up to work around issues. Interpolation is turned for 12G otherwise it is off. Can increase interpolation, can turn on 8 dB equalization (troubleshooting). Vseries can use 4 channel SE connectionand at 40GSa/s we are at a 16GHZ bw. Conflicts with bw of hdmi2.1? Looks for SSB byte within 10 bits… SSBs may be greater and this can be increased to 30.
HFR1-5	Data rate accuracy	TP1	LTP3	Ltp3 waveform (clock), average of period/2 ppm
HFR1-6	Data jitter RJ 1MUI	TP1	LTP3	Ltp3 waveform, non tested lanes are quiet. Standard jitter ezjit…narrow bandwidth vs wide and why we end up taking a hit against tek. Used for mask expansion in hfr1-7
HFR1-7	Data eye 2MUI	TP2EQ	LTP5-8	Ltp5-8 pattern all four lanes transmitting and store each lane**… crosstalk** of test fixture is included in the captures and then we use s16p file to create data eye for each lane using the other 3 as interferers. Expand mas to go from 1e-6 to 1e-10BER. We use CTLE(8dB) and DFE (ctle combined with cable model). Short cable model with 1 dB ctle also. At 80G sample rate a 12 G signal may have odd dots all over the eye. If user can go to config and turn on 2 point interpolation and problem goes away.
HFR1-8	Ac common mode	TP1	LTP5-8	non tested lanes are quiet. SE connection, standard cm calculation and measurement is peak to peak voltage limit-150mV usually get 50 to 100mv.
HFR1-9	FFE (optional)	TP1	LTP4	, measuring pre shoot and, de-emphasis and there are two methods to do that and **customer must know** what their chip can do. FFE method type. customer needs to know if dut does it or not. Often confused because waveform will look like it is augmented (and is) but control does NOT exist for the DUT.

HDMI 2.1 Source Eye Diagram Test

LINK TRAINING PATTERN

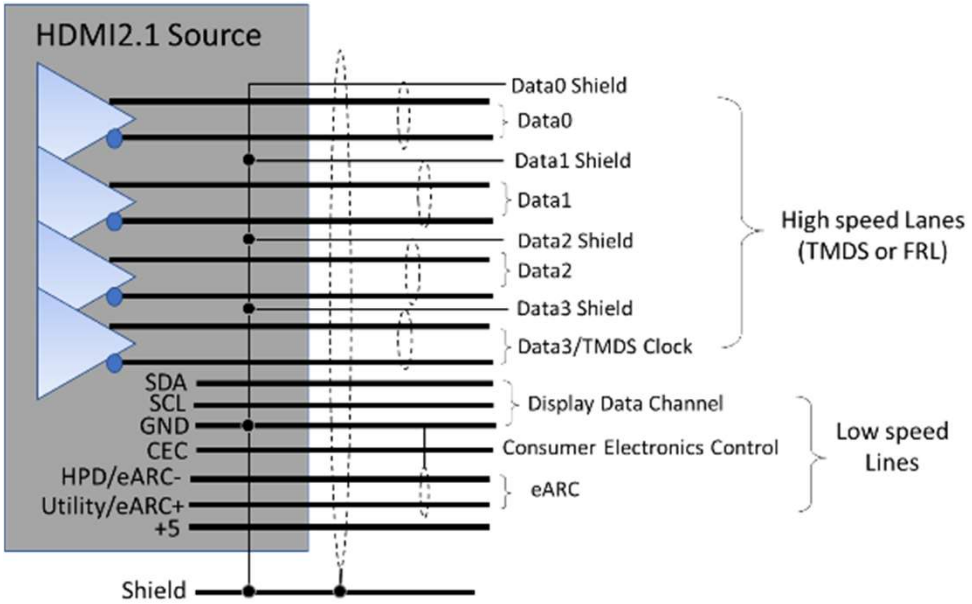
Testing for Eye diagram and jitter includes crosstalk of other data lanes as manifest in the cable model we use for HDMI 2.1: WCM3 (worst case) and SCM3 (short)

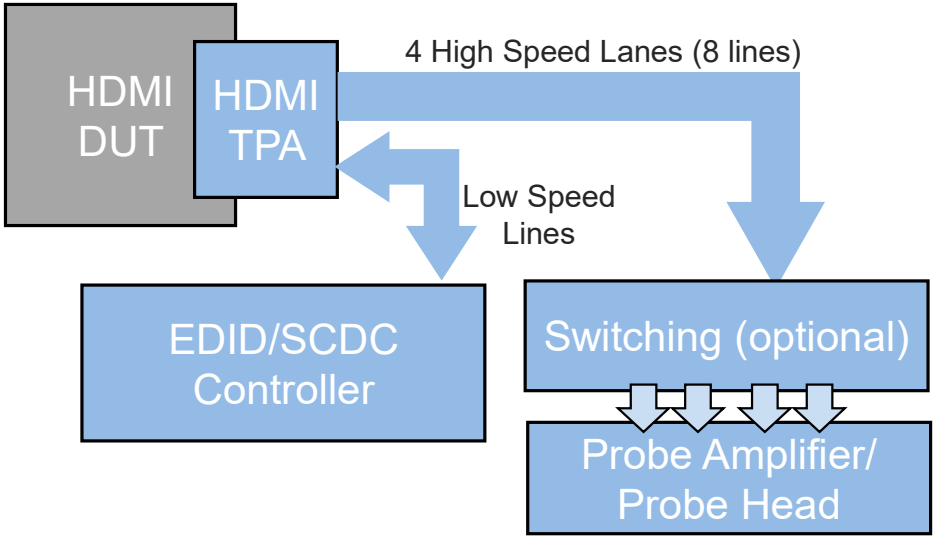
Process:
Acquire and store D0, D1, D2, D3 waveforms.
Render D0 TP2 eye:
D0&cable s4pD0->D0 + D1& xtalk s4p D1->D0 +
D2& xtalk s4pD2->D0 +D3& xtalk s4pD3->D0

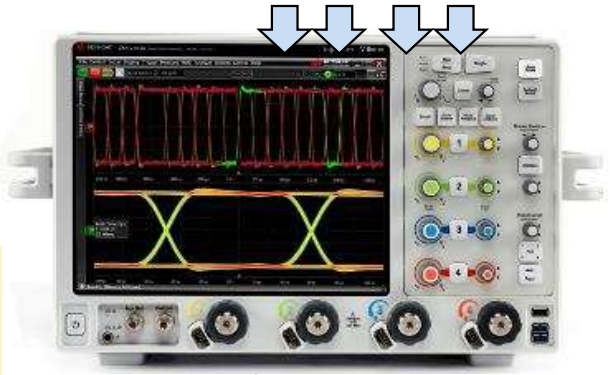


With exception of Inter-pair skew, FRL is tested one lane at a time.

HDMI 2.1 Source Physical Layer Test Overview







Four Channel scope

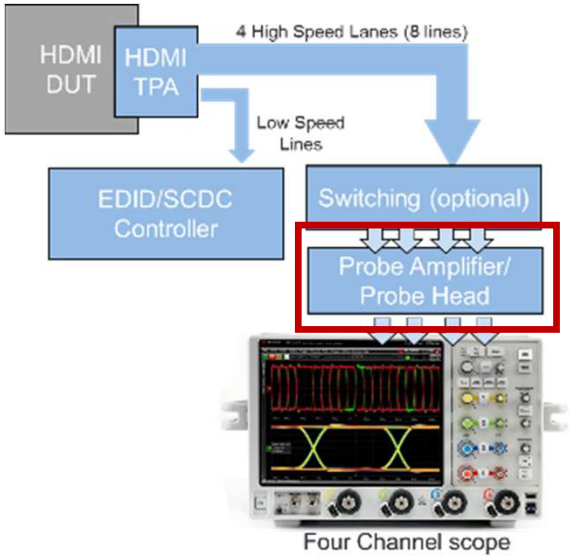
HDMI Interface
-High speed lanes to be measured
-Low speed lanes for control and status

HDMI 2.0 no longer exists. It is referred to as ‘HDMI2.1 TMDS’.
HDMI 2.1 Fixed Rate Link (FRL) now operates 3, 6, 8, 10, 12Gbs and supports 3 &4 lane operation at 3 and 6 and 4 lane operation for 8, 10, 12 Gbs

Probe Amplifier/Probe Heads

HDMI 2.1 Source measurement requires:

1. **Terminating tested and untested lanes into 50 ohms pulled up to 3.3 volts.**
2. **Single-ended acquisitions for single-ended and differential parameter measurements**
3. **Bandwidth appropriate for HDMI version and test**
   a. HDMI1.4: 8GHz
   b. HDMI2.1 TMDS (HDMI2.0): 13GHz [16GHz recommended]
   c. HDMI2.1 FRL: 20GHz
4. **Lane connections supporting minimum of 2 at a time**

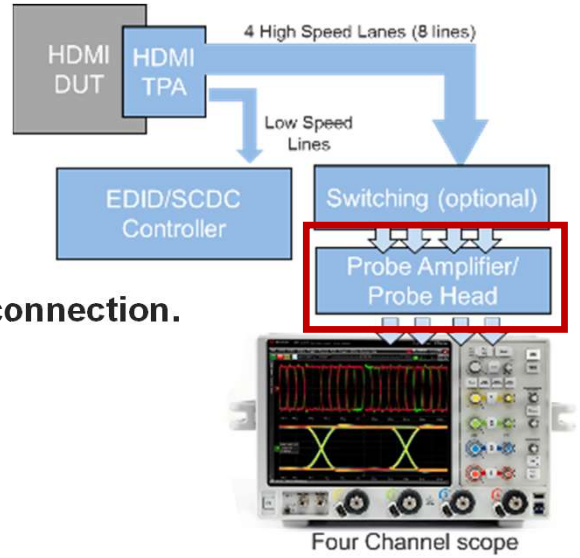


Many HDMI devices on market can operate into 50ohm termination to ground, but the official requirement is 50 ohms to Vterm=3.3v. Some differential measurements are TP2Eq which incorporates a cable model and equalization. For these, a single-ended acquisition is required because there is SE->Diff mode conversion that exists in the cable model.
HDMI 2.0/2.1 compliance testing did not specify a bandwidth. Keysight suggested 13GHz as a minimum, Tektronix indicated 12.5GHz was allowable 'in a pinch'. For accurate rise time measurement margin above rise time of DUT+fixture is recommended; 16GHz is appropriate for devices close to rise time specification
2 lanes at a time is required for HDMI 2.1 TMDS Eye diagram and Inter-pair Skew test.

Probe Amplifier/Probe Heads continued

Keysight has many solutions for probing…

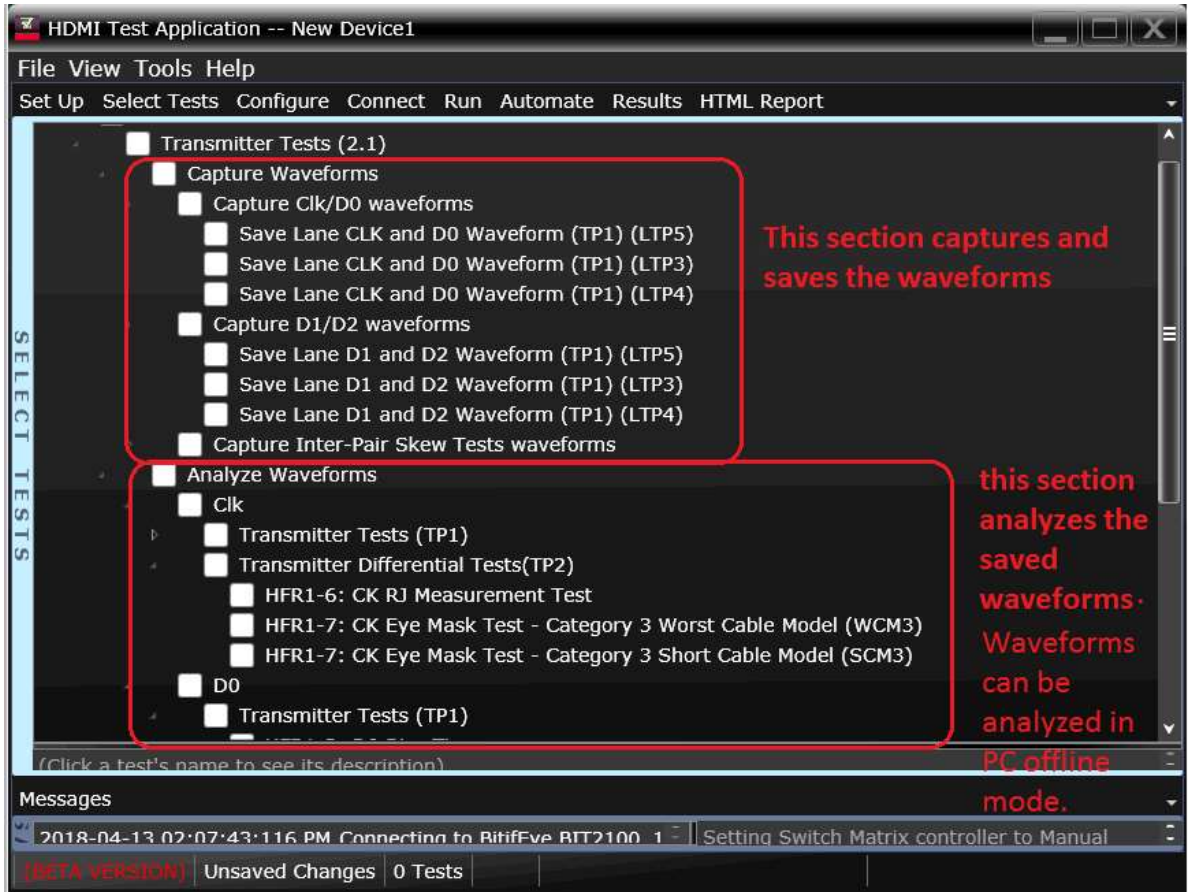
	Probe/Amp	Rationale
1.	1169B/N5380B	HDMI 1.4/HDMI2.1TMDS w T_{rise} high
2.	N7010A Active Termination Adapter	Low Cost & Noise, High BW, Ease of connection.
3.	N280xA/N5444A InfiniiMaxIII	Highest bandwidth
4.	N7003A/N5444A InfiniiMode	Internal switch enables productivity



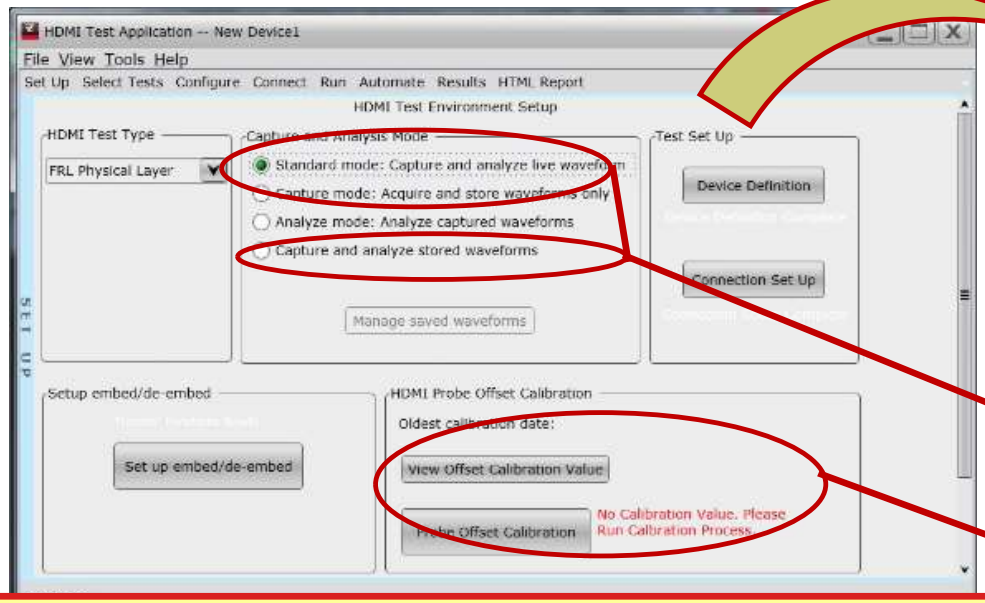
1169B/N5380B requires power supply routing to N5380B. 1169B/N5380B Bandwidth is marginal for HDMI2.1 TMDS. The active termination adapter is a single-ended device with specific purpose to pull up to a termination voltage. When N7010A is implemented, unused lanes must have proper termination.
The N2800A series is very high end and may be chosen for other technologies. For HDMI only, the N7003A would be preferred. The N7003A has A, B, A-B and (A+B/2) positions. In the HDMI application ONLY A or B are used, thus using the N7003A capability as a switch. It does not preclude ability of user to troubleshoot in other modes.

HDMI 2.1 Source Compliance Test software: D9021HDMC

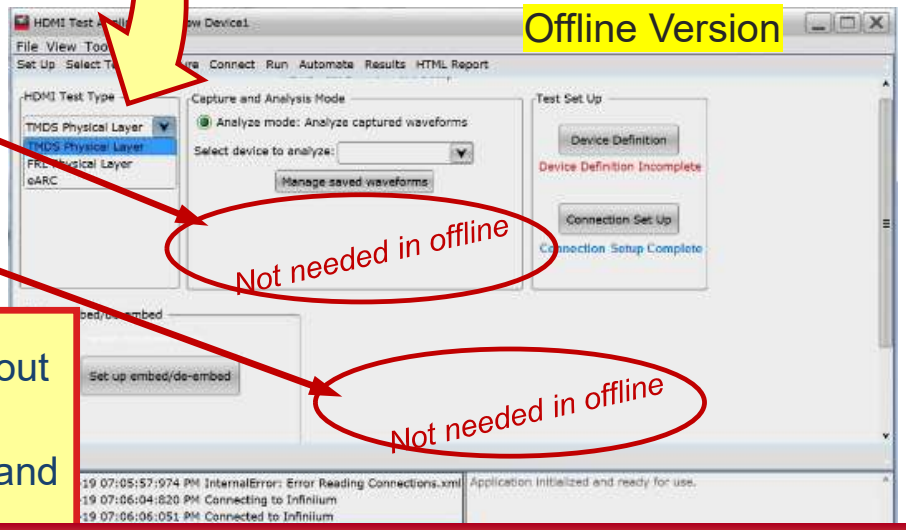
Modes of Operation: Capture and Analysis



HDMI 2.1 Compliance testing Offline



Infiniium Offline: N8900A-001
SDA Package: N8900A-002
Analysis Package: N8900A-003



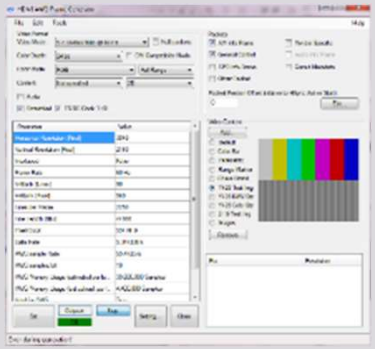
You can now DOUBLE HDMI test productivity without buying a second scope!!!
Requires laptop/PC, Infiniium Offline license and packages and an HDMI license.
For 10% more you can get 2x throughput!!!
Consider it as schedule insurance!!

Now available on Infiniium Offline with FULL features!

Sink Test

Sink Phy Layer

M8195A AWG + infrastructure



Approved MOIs

N5991HP1A Compliance Software

BitifEye Digital Test Solutions

HDMI Plug TPA

EDID/SCDC Controller

Sink Tests

FRL AND TMDS

Sink Tests (FRL):

- Test ID HFR2-1: Max Differential Swing Tolerance
- Test ID HFR2-2: Intra-Pair Skew
- Test ID HFR2-3: Inter-Pair Skew
- Test ID HFR2-4: Minimum Link Rate Tolerance
- Test ID HFR2-5: Jitter Tolerance

Sink Tests (TMDS):

- Test ID HF2-1: Min/Max Differential Swing Tolerance
- Test ID HF2-2: Intra-Pair Skew
- Test ID HF2-3: Jitter Tolerance

Sink Testing

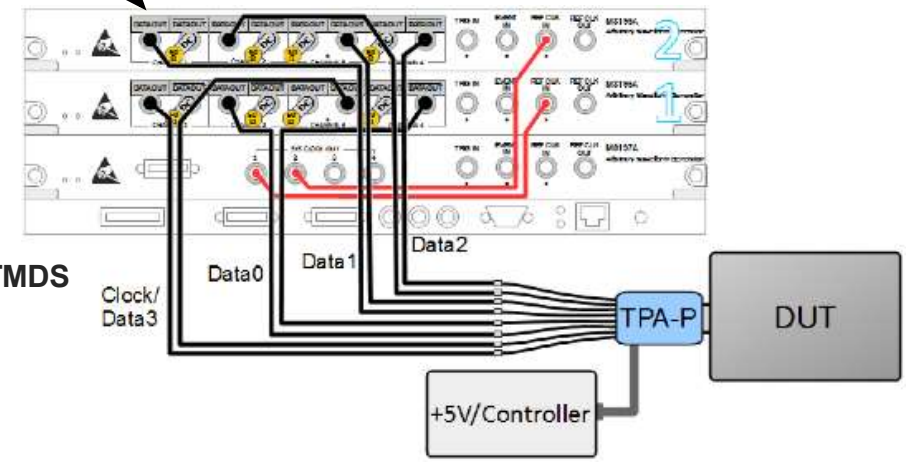
- All Receiver tests have the same measurement-
  - ✓ **A disparity error count from the DUT**
- The Input conditions vary: Level, Intra-Pair skew, Inter-Pair Skew, Link Rate, Jitter

Sink Tests (FRL):

- Test ID HFR2-1: Min/Max Differential Swing Tolerance
- Test ID HFR2-2: Intra-Pair Skew
- Test ID HFR2-3: Inter-Pair Skew
- Test ID HFR2-4: Minimum Link Rate Tolerance
- Test ID HFR2-5: Jitter Tolerance

- **Level:** Setting in AWG for both signal **and** complement
- **Intra Pair Skew**: …. VERY clever!
- **Inter Pair Skew**: AWG waveform delay value
- **Link Rate**: AWG waveform frequency parameter
- **Jitter tolerance**: jitter cocktail ++

Item	Generic Equipment Function	Keysight Equipment
1	TMDS Signal Generator	Keysight M8195A based test platform: • Quantity 2 Keysight M8195A Arbitrary Waveform Generators, opt. 002, 16G, SEQ • Quantity 1 Keysight M8197A Multi-Channel Synchronization Module for M8195A • Quantity 1 Keysight M9505A AXIe 5 slot Chassis • Quantity 4 Keysight N4871A matched pair co-axial cables • Quantity 8 SMA DC blocks • Quantity 4 SMA 50 Ohm Terminations • Quantity 1 Oscilloscope for calibration purposes (13GHz or more recommended):
		Equipped with:



Sink Test

- All Receiver tests have the same measurement-
  - ✓ **A disparity error count from the DUT**
- Jitter Tolerance: jitter cocktail ++ : RJ, PJ, ISI, ISI++

Sink Tests (FRL):

- Test ID HFR2-1: Min/Max Differential Swing Tolerance
- Test ID HFR2-2: Intra-Pair Skew
- Test ID HFR2-3: Inter-Pair Skew
- Test ID HFR2-4: Minimum Link Rate Tolerance
- Test ID HFR2-5: Jitter Tolerance

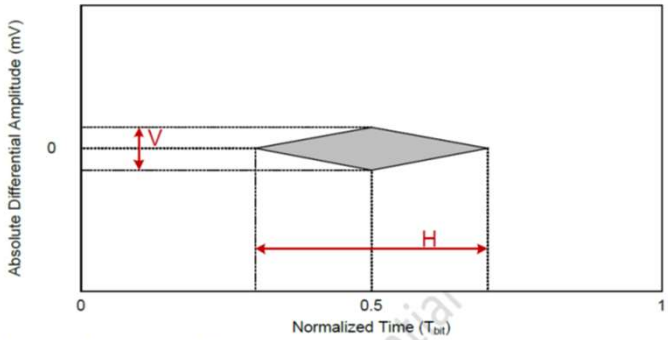
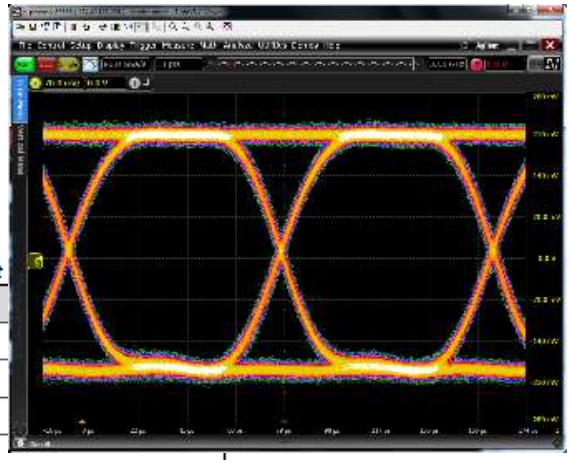


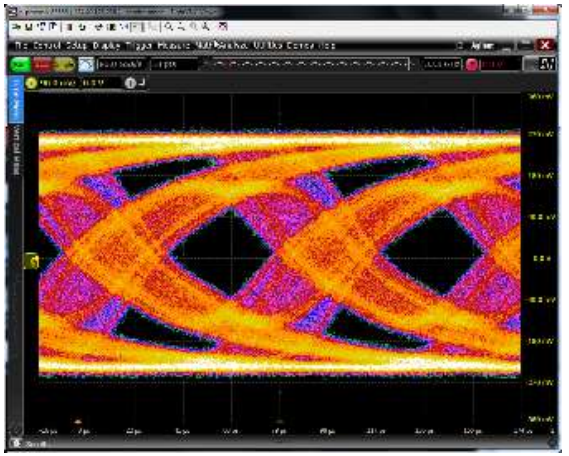
Figure 6-11: Eye diagram at TP2_EQ¹

Tab... ...liagram at

FRL Bit Rate, R_{bit}	H (T_{bit})	V (mV)
3 Gbps	0.5	150
6 Gbps	0.4	150
8 Gbps	0.385	135
10 Gbps	0.37	120
12 Gbps	0.35	100



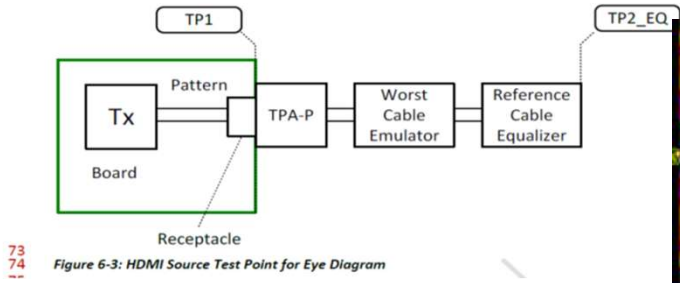
12Gbps clean signal



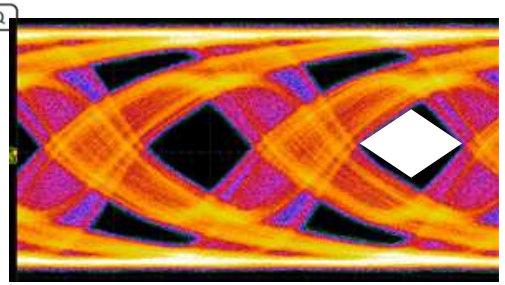
12Gbps signal with ISI and Jitter

Sink Test

- All Receiver tests have the same measurement-
  - ✓ **A disparity error count from the DUT**
- Jitter Tolerance: jitter cocktail ++ : RJ, PJ, ISI, ISI++



73
74
Figure 6-3: HDMI Source Test Point for Eye Diagram



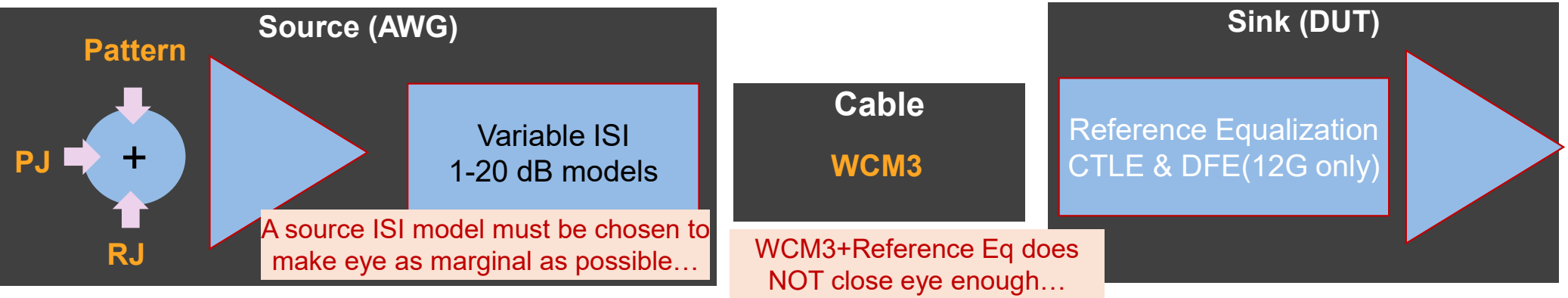
Sink Tests (FRL):

- Test ID HFR2-1: Min/Max Differential Swing Tolerance
- Test ID HFR2-2: Intra-Pair Skew
- Test ID HFR2-3: Inter-Pair Skew
- Test ID HFR2-4: Minimum Link Rate Tolerance
- Test ID HFR2-5: Jitter Tolerance

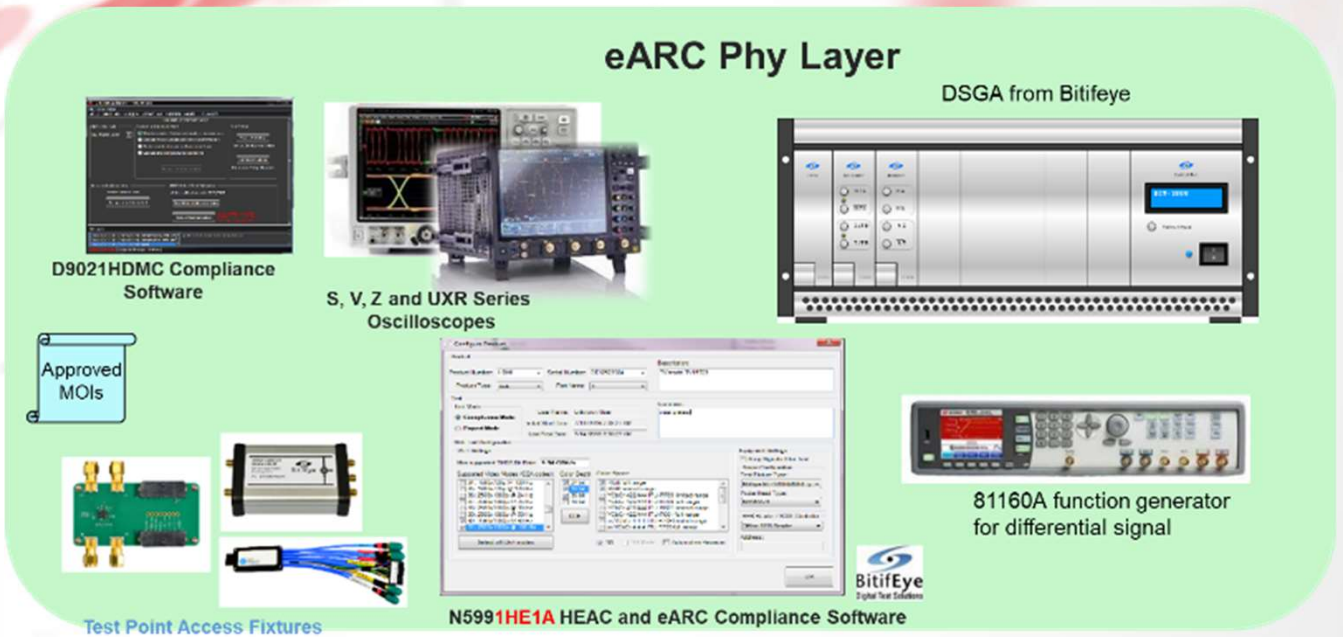
This mask is EXPANDED by AWG PN, σ_{AWG}

The RJ from AWG is NOT gaussian and since AWG repeats does not go beyond 1e-6 BER.

rms RJ becomes $(0.2*T_{bit} - 3.2*\sigma_{AWG\_PN}) / 9.784$ for 1 million accumulated transition edges.



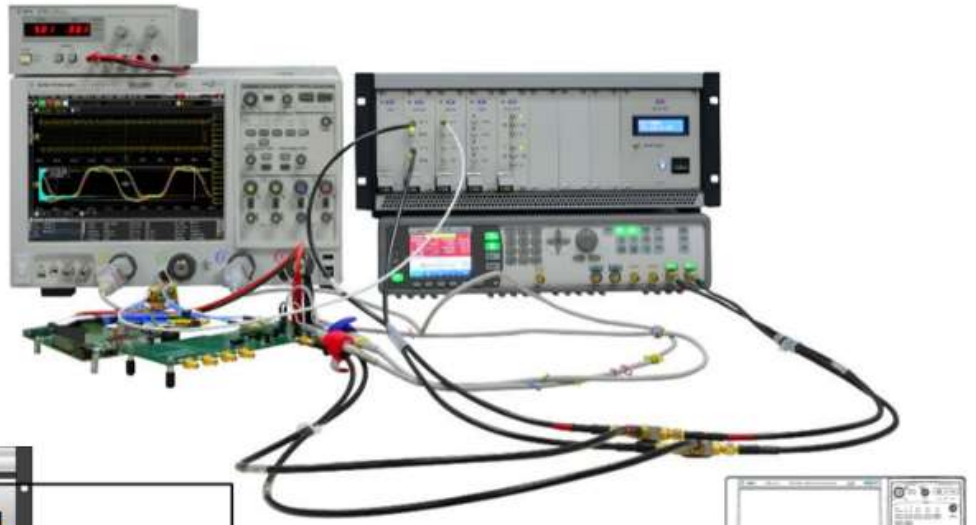
eARC


eARC Phy Layer
DSGA from Bitifeye
D9021HDMC Compliance Software
S, V, Z and UXR Series Oscilloscopes
Approved MOIs
81160A function generator for differential signal
Test Point Access Fixtures
N5991HE1A HEAC and eARC Compliance Software
BitifEye

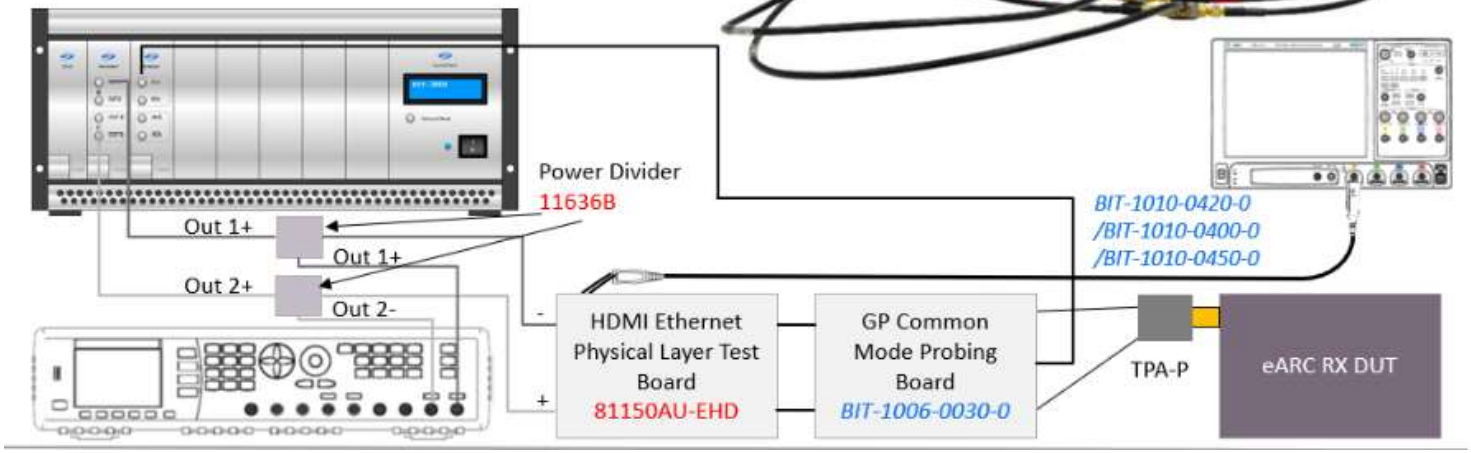
eARC use model

eARC RX Setup

eARC RX Tests		
HFR5-2-1	Source	eARC RX Termination Supply Voltage Tolerance at TP2 (VEH_eARC)
HFR5-2-2	Source	eARC RX Differential Mode Swing Tolerance at TP2 (VeARC_SWING_DM2)
HFR5-2-4	Source	eARC RX Differential Bit Rate Tolerance at TP1 (ReARC_BIT_AUDIO)
HFR5-2-5	Source	eARC RX Differential Mode Eye Diagram Tolerance at TP1
HFR5-2-6	Source	eARC RX Differential Mode Duty Cycle Tolerance at TP1 (DeARC_DM1)
HFR5-2-7	Source	eARC RX Common Mode Output Data Bit Time at TP1 (TeARC_BIT_CM)
HFR5-2-8	Source	eARC RX Common Mode Output "1" Bit Toggle Time at TP1 (TeARC_TGL_CM)
HFR5-2-9	Source	eARC RX Common Mode Input Swing Tolerance at TP1 (UeARC_MASTER_SWING_CM1)
HFR5-2-10	Source	eARC RX Common Mode Output Swing at TP1 (UeARC_SLAVE_SWING_CM1)
HFR5-2-12	Source	eARC RX Common Mode Output Rise/Fall Time (10% - 90%) at TP1 (TeARC_RISE_FALL_CM)

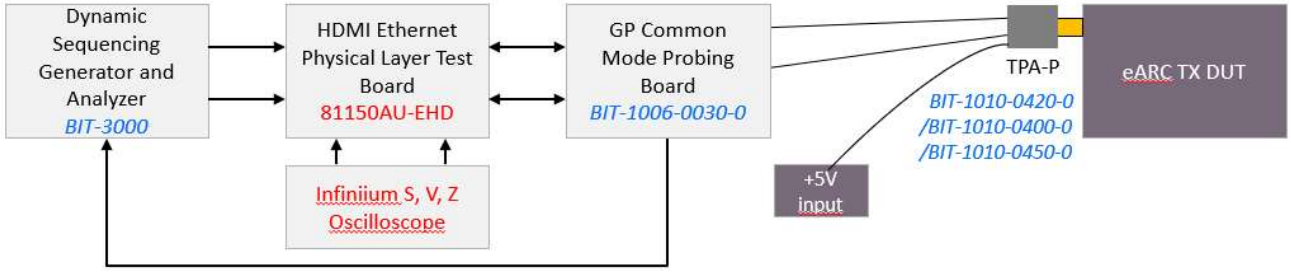


- Oscilloscope for calibration
- 81160A function generator for Diff signal
- DSGA for CM signal
- Offered by Keysight
- Offered by BitifEye



eARC TX Setup

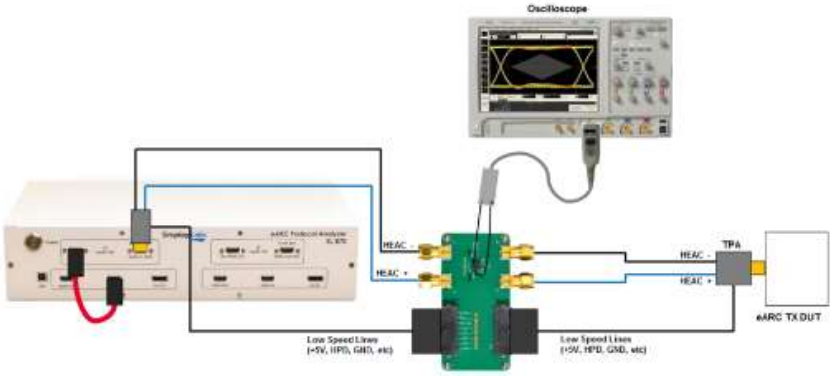
HFR5-1-10	Sink	eARC TX Common Mode Output Data Bit Time at TP2 (TeARC_BIT_CM)
HFR5-1-11	Sink	eARC TX Common Mode Output "1" Bit Toggle Time at TP2 (TeARC_TGL_CM)
HFR5-1-12	Sink	eARC TX Common Mode Output Swing at TP2 (UeARC_MASTER_SWING_CM2)
HFR5-1-13	Sink	eARC TX Common Mode Input Swing Tolerance at TP2 (UeARC_SLAVE_SWING_CM2)
HFR5-1-15	Sink	eARC TX Common Mode Output Rise/Fall Time (10% - 90%) at TP2 (TeARC_RISE_FALL_CM)



3rd party equipment by Simplay labs required

- SL870 Protocol Analyzer

eARC TX Tests		
HFR5-1-1	Sink	eARC TX Termination Supply Voltage at TP2 (VEH_eARC)
HFR5-1-2	Sink	eARC TX Differential Mode Swing at TP2 (VeARC_SWING_DM2)
HFR5-1-4	Sink	eARC TX Differential Bit Rate at TP2 (ReARC_BIT_AUDIO)
HFR5-1-5	Sink	eARC TX Differential Mode Rise/Fall Time at TP2 (TeARC_DM2_RISE_FALL)
HFR5-1-6	Sink	eARC TX Differential Mode Clock Jitter at TP2 (TeARC_DM2_CLK_JITTER)
HFR5-1-7	Sink	eARC TX Differential Mode Eye Diagram at TP1
HFR5-1-8	Sink	eARC TX Differential Mode Duty Cycle at TP1 (DeARC_DM1)
HFR5-1-9	Sink	eARC TX Differential to Common Mode Conversion at TP2 (VeARC_DM2_CM_CONV)

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